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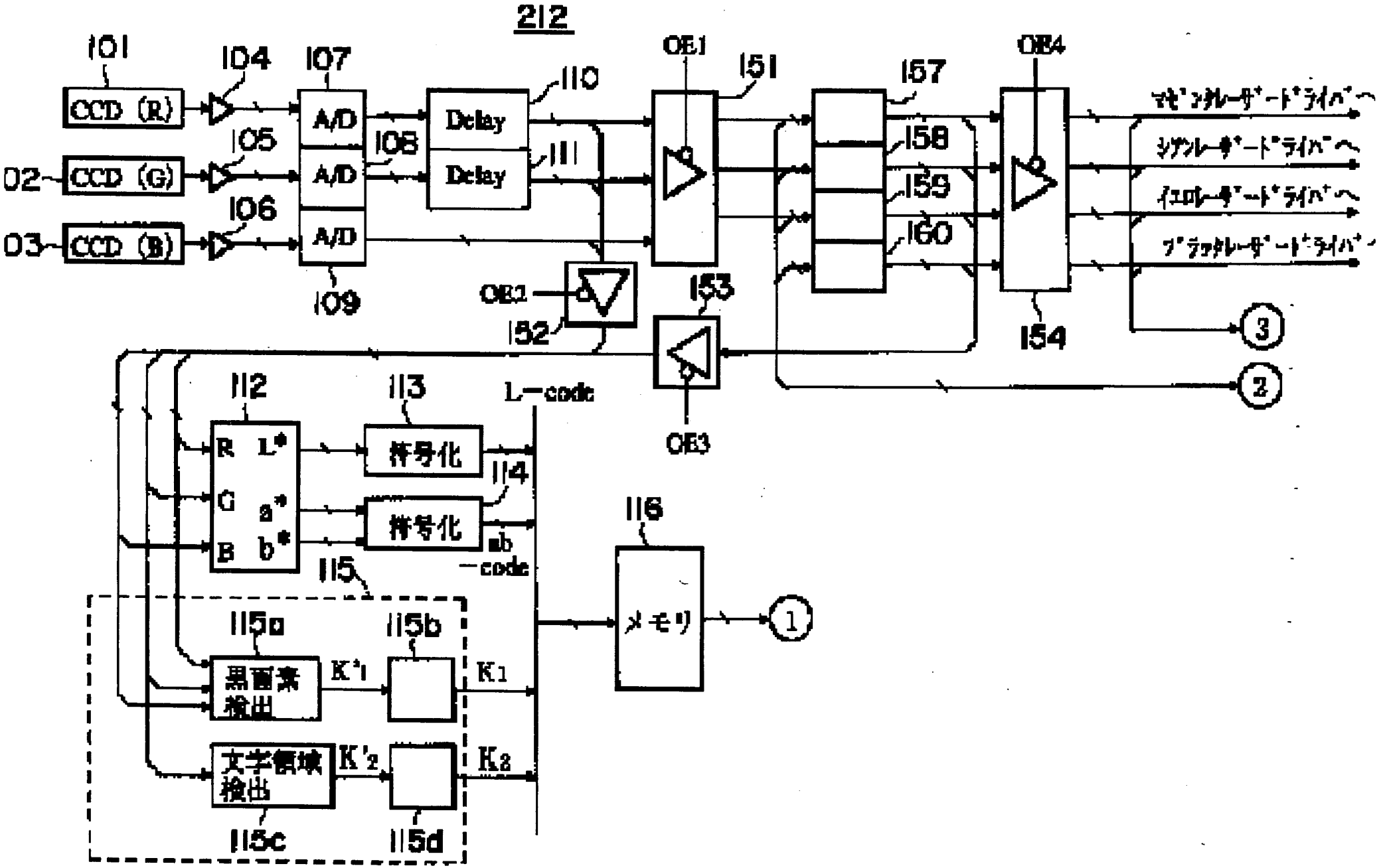
**Titel:** METHOD AND DEVICE FOR PROCESSING PICTURE

## Zusammenfassung

**PURPOSE:** To dissolve the roughness of the encoded and decoded reproducing pictures of input pictures, a dot picture area for instance, and to improve picture reproducibility by operating so as to perform encoding nonlinearly for the DC components of chromaticity information at the time encoding inputted full-color picture signals.

**CONSTITUTION:** A color space converter 112 converts RGB signals into a luminance signal L* and chromaticity signals a* and b*. Then, the encoder 113 of the luminance signal L* encodes the L* signal by the picture element unit of 4×4 and outputs an encoded signal L-code and the encoder 114 of the chromaticity signals encodes the a* and b* signals by the picture element block unit of 4×4 and outputs the encoded signal ab-code. Since the inputted full-color picture signals are separated into luminance information and the chromaticity information for each prescribed unit and are encoded and the DC components of the chromaticity information are nonlinearly encoded especially in such a manner, the encoding is performed more efficiently.


212
101
CCD (R)
102
CCD (G)
103
CCD (B)
104
105
106
107
A/D
A/D
A/D
108
109
Delay
Delay
110
111
OE1
151
152
OE2
153
OE3
157
158
159
160
OE4
154
マゼンタレーザードライバへ
シアンレーザードライバへ
イエローレーザードライバへ
ブラックレーザードライバへ
3
2
112
R L*
G a*
B b*
113
符号化
114
符号化
ab
−code
L−code
115
115a
黒画素
検出
K'1
115b
K1
文字領域
検出
K'2
K2
115c
115d
116
メモリ
1

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates full color image data to the image-processing technique of performing processing of coding (compression) and a decryption (extension), and its equipment, about the image-processing technique and its equipment.
[0002]
[Description of the Prior Art] Conventionally, the equipment currently indicated by Japanese Patent Application No. 141826 [ 63 to ] etc. is proposed as equipment which divides full color image data into a lightness information and a chromaticity information for every predetermined pixel block, and is encoded (compression).
[0003] In such a compression method, the alternating current component of a chromaticity information was encoded per 4 pixel x four lines using the functionality of a lightness information and a chromaticity information, for example. Furthermore, the attribute of image information is classified into two according to the characteristic feature of image information, and different coding is performed according to it.
[0004]
[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional example, since the functionality of a lightness information and a chromaticity information was weak in the case of the manuscript which forms arbitrary picture images macroscopically in the combination of the artificial pattern in pixel unit level like a half-tone-dot picture image, there was a problem that the repeatability of the picture image encoded and decrypted became bad. Especially, the attribute of a lightness information was not correctly classified according to the fraction of a highlight, but since optimum coding was not performed, there was a fault that a degradation of quality of image will become large.
[0005] For example, since the chromaticity of a half tone dot completely differs from the chromaticity of the ground of manuscript paper in the case of a half-tone-dot manuscript, the picture image area which looks macroscopic to monotonous **** will also be judged to be the same area as the character section etc. Therefore, coding with little amount of information assigned to the dc component of a chromaticity is chosen, and a false profile occurs, or the fraction of a highlight ill-behaved-results and carries out.
[0006] Even if this invention encodes and decrypts the picture image formed so that it might be made in view of the above-mentioned conventional example and it might become arbitrary picture images macroscopically in the combination of the artificial pattern in pixel unit level, it aims at offering the image-processing technique with sufficient repeatability and its equipment of a picture image.
[0007]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the image-processing technique of this invention consists of the following processes. Namely, the input process which is the image-processing technique of processing a full color picture signal, and inputs a full color picture signal, The split process which divides into a predetermined unit the full color picture signal which carried out [ above-mentioned ] the input, The separation process which divides the above-mentioned full color picture signal into a lightness information and a

chromaticity information, The lightness information on the above-mentioned full color picture signal is divided into a dc component and an alternating current component for every above-mentioned predetermined unit. A quantization and the quantization process to encode, The 1st calculation process which computes the amplitude of the alternating current component of the above-mentioned lightness information in the above-mentioned predetermined unit, The 2nd calculation process which computes the amplitude of the alternating current component of the above-mentioned chromaticity information in the above-mentioned predetermined unit, It has the image-processing technique characterized by having the 1st coding process which computes the ratio of the amplitude of the alternating current component of the above-mentioned lightness information to the amplitude of the alternating current component of the above-mentioned chromaticity information, and is encoded, and the 2nd coding process which encodes the dc component of the above-mentioned chromaticity information nonlinear.

[0008] Moreover, an input means according to other invention to be the image processing system which processes a full color picture signal, and to input a full color picture signal, A split means to divide into a predetermined unit the full color picture signal which carried out [ above-mentioned ] the input, A separation means to divide the above-mentioned full color picture signal into a lightness information and a chromaticity information, The lightness information on the above-mentioned full color picture signal is divided into a dc component and an alternating current component for every above-mentioned predetermined unit. A quantization and the quantization means to encode, A 1st calculation means to compute the amplitude of the alternating current component of the above-mentioned lightness information in the above-mentioned predetermined unit, A 2nd calculation means to compute the amplitude of the alternating current component of the above-mentioned chromaticity information in the above-mentioned predetermined unit, It has the image processing system characterized by having a 1st coding means to compute the ratio of the amplitude of the alternating current component of the above-mentioned lightness information to the amplitude of the alternating current component of the above-mentioned chromaticity information, and to encode, and a 2nd coding means to encode the dc component of the above-mentioned chromaticity information nonlinear.

[0009]

[Function] The picture signal is divided into a lightness information and a chromaticity information in the case of coding of the full color picture signal which inputted this invention by the above configuration, and it operates so that it may encode nonlinear about the dc component of a chromaticity information.

[0010]

[Example] With reference to an accompanying drawying, the suitable example of this invention is explained in detail below.

[0011] [Equipment schema explanation ( drawing 1 )] view 1 is the block diagram showing the schema configuration of the full color copying machine which is the typical example of this invention. In drawing 1 , 201 is manuscript base glass and the manuscript 202 which should be read is placed. A manuscript 202 is irradiated with the light source 203, it passes through mirrors 204-206, and an image is tied on CCD208 by optical system 207. Furthermore, by the motor 209, the mirror unit 210 containing a mirror 204 and the light source 203 is mechanically driven at a speed (V), the 2nd mirror unit 211 containing a mirror 205,206 is driven at speeds 1/2V, and the whole surface of a manuscript 202 is scanned. 212 is the image-processing circuit section and is a fraction which processes the read image information as an electrical signal, and is outputted as a print signal.

[0012] 213-216 are semiconductor laser, it drives with the print signal outputted from the image-processing circuit section 212, and the laser beam which emitted light by each semiconductor laser forms a latent image on a photoconductor drum 225-228 by the polygon mirrors 217-220. 221-224 are the development machines for developing a latent image with the toner of black (Bk), yellow (Y), cyanogen (C), and a Magenta (M) respectively, the toner of each developed color is imprinted by the form and a full color printed output is made.

[0013] The form cassettes 229-231 and the form to which **** and paper was fed from either of

the trays 232 pass through the resist roller 223, and on the imprint belt 234, it adsorbs and they are conveyed. The timing of feeding and a synchronization are taken, the toner of each color is beforehand developed by photoconductor drums 225-228, and a toner is imprinted by the form with conveyance of a form.

[0014] The form with which the toner of each color was imprinted is separated / conveyed, and a form is fixed to a toner and it is delivered to the delivery tray 236 by the fixing assembly 235.

[0015] [Schema explanation [ of an image-processing circuit ] ( drawing 2 - view 3 )] view 2 - view 3 is the block diagram showing the configuration of the image-processing circuit 212. In drawing 2 - view 3 , 101-103 are red (R), green (G), and CCD sensor of blue (B) respectively, and the output from each sensor is amplified by the corresponding analog amplifiers 104-106, and is respectively outputted by the corresponding A/D converter as a digital signal. 110 and 111 are delay memory respectively and rectify the spatial gap between three CCD sensors 101-103.

[0016] 151-156 are the gate circuits of try ******** respectively, and only when OE [ which is set as CPU (un-illustrating) shows to Table 1 according to the content of variable power processing ]1, - OE6 signal is "0", they output the inputted signal. 157-160 are variable power circuits respectively, and carry out variable power of the picture signal in the orientation of horizontal scanning.

[0017] 112 is a color space conversion machine and changes an RGB code into a lightness signal (L*) and a chromaticity signal (a* and b*). Here, they are L*, a*, and b*. A signal is L*, a*, and b* as an international canonical at CIE. As space, it is a signal showing the chromaticity component specified, and they are L*, a*, and b*. A signal is calculated according to a formula (1).

$$\begin{bmatrix} L^* \\ a^* \\ b^* \end{bmatrix} = \begin{bmatrix} 0 & \alpha_{12} & 0 \\ \alpha_{21} & \alpha_{22} & 0 \\ 0 & \alpha_{32} & \alpha_{33} \end{bmatrix} \begin{bmatrix} (X/X_0)^{1/3} \\ (Y/Y_0)^{1/3} \\ (Z/Z_0)^{1/3} \end{bmatrix} + \begin{bmatrix} \alpha_{14} \\ 0 \\ 0 \end{bmatrix} \quad \cdots\cdots (1)$$

Here, they are alphaij, X0, Y0, and Z0. It is a constant.

[0018] Moreover, X, Y, and Z are signals which calculate by the RGB code and occur, and are expressed with a formula (2).

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} \beta_{11} & \beta_{12} & \beta_{13} \\ \beta_{21} & \beta_{22} & \beta_{23} \\ \beta_{31} & \beta_{32} & \beta_{33} \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad \cdots\cdots (2)$$

Here, betaij is a constant.

[0019] It is the coding machine of a lightness signal and 113 is L*. A signal is encoded per pixel block of 4x4, the coded signal (L-code) is outputted, 114 is the coding machine of a chromaticity signal, and they are a* and b*. A signal is encoded per pixel block of 4x4, and the coded signal (ab-code) is outputted.

[0020] Black pixel detector 115a which generates the judgment signal (K1') of whether 115 is a feature-extraction circuit and the concerned pixel is a black pixel, 4x4 area processing circuit 115b which inputs a judgment signal (K1') and judges whether the inside of a pixel block of 4x4 is a black pixel area, And character area detector 115c and the judgment signal (K2') which generate the judgment signal (K2') of whether the concerned pixel is in a character area are inputted, and it consists of 115d of the 4x4 area processing circuits which judge whether the inside of a pixel block of 4x4 is a character area.

[0021] 116 is an image memory and the coded signal (L-code) of a lightness information, the coded signal (ab-code) of a chromaticity information, the judgment signal (K1) which it is as a result of a feature extraction, and a judgment signal (K2) are stored.

[0022] 141-144 are the concentration signal generation circuits for a Magenta (M), cyanogen (C), yellow (Y), and blacks (Bk) respectively, and take the almost same configuration.

[0023] 117a, 117b, 117c, and 117d are L* by the coded signal (L-code) which is the decryption machine of a lightness information and was read from the image memory 116. It is a* by the coded signal (ab-code) which decrypted the signal, and 118a, 118b, 118c, and 118d are the

decryption machines of a chromaticity information, and was read from the image memory 116. A signal and b* The decode of the signal is carried out.
[0024] 119a, 119b, 119c, and 119d are L* which is a color space conversion machine and was decrypted, a*, and b*. It is the conversion circuit which changes a signal into the Magenta (M) which is a toner-development color, cyanogen (C), yellow (Y), and each color component of black (Bk). 120a, 120b, 120c, and 120d are concentration conversion circuits, and consists of a lookup table (henceforth LUT) of ROM or RAM. 121a, 121b, 121c, and 121d are spacial filters, and rectifies spatial frequency of an output picture image. Moreover, 122a, 122b, 122c, and 122d are pixel correction circuits, and rectifies the decrypted image data.
[0025]
[Table 1]

| | 拡大処理の場合 (第1のモード) | 拡大処理の場合 (第1のモード) |
|---|---|---|
| OE1 | 0 | 1 |
| OE2 | 1 | 0 |
| OE3 | 0 | 1 |
| OE4 | 1 | 0 |
| OE5 | 1 | 0 |
| OE6 | 0 | 1 |

[Lightness component coding machine 113 ( drawing 4 - view 14 )] view 4 is the block diagram showing the configuration of the lightness information coding machine 113. Moreover, drawing 5 - view 6 is drawing showing flowing of lightness information coding notionally.
[0026] Here, coding (compression) of image data is performed as a 1-block unit in a total of 16 pixels of 4 pixel (orientation of horizontal scanning) x4 line (the orientation of vertical scanning), as shown in drawing 7 . In drawing 7 , XPHS is a 2-bit signal which shows a horizontal-scanning position, the signal of "0", "1", "2", and "3" which shows a value is outputted repeatedly, YPHS is a 2-bit signal which shows a vertical-scanning position, and the signal of "0", "1", "2", and "3" which shows a value is outputted repeatedly. Synchronizing with these signals, 1 block of 4 pixel x4 line is started.
[0027] First, drawing 5 - view 6 is explained with reference to the idea of lightness information coding. If the Hadamard transform of four line x4 train shown in (3) formulas is given to this when the started 1-block lightness information is set to Xij (i, j=1-4), as shown in 401 of drawing 5 , a matrix (Yij (i, j=1-4)) which is shown in 402 of drawing 5 will be acquired. A Hadamard transform is a kind of orthogonal transformation, the data of four line x4 train are developed by the 2-dimensional Walsh function, and the signal of a time domain or a space area is equivalent to changing into a frequency domain or a spatial-frequency area with Fourier transformation. That is, the matrix after a Hadamard transform (Yij (i, j=1-4)) serves as the signal equivalent to each component of spatial frequency which the matrix (Xij (i, j=1-4)) of an input signal has.
[0028]

$$\begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} = (1/4) \cdot H^{t} \begin{bmatrix} X_{11} & X_{12} & X_{13} & X_{14} \\ X_{21} & X_{22} & X_{23} & X_{24} \\ X_{31} & X_{32} & X_{33} & X_{34} \\ X_{41} & X_{42} & X_{43} & X_{44} \end{bmatrix} \cdot H$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{bmatrix} \quad \cdots\cdots\cdots (3)$$

H is the Hadamard matrix of 4x4 here, and it is HT. It is the transposed matrix of H.
[0029] Now, like the case of 2-dimensional Fourier transformation, in the output matrix (Yij (i, j=1-4)) of this Hadamard transform, the more the value (namely, line number) of i becomes large, the component of the high spatial frequency of the orientation of vertical scanning is arranged, and the more the value (namely, train position) of j becomes large, the more the component of the high spatial frequency of the orientation of horizontal scanning is arranged. Especially, in i=j=1, it becomes with Yij=(1/4) sigmaXij, and the dc component of input data Xij (i, j=1-4), i.e., the signal equivalent to the average, (strictly signal 4 times the value of the average) is outputted.
[0030] Furthermore, as for the picture image generally read, it is known with the reading resolution of reading sensors, such as CCD, the transparency property of optical system, etc. that it is not few to the thing of a high spatial-frequency component. A matrix which forms the signal Yij (i, j=1-4) after a Hadamard transform into a scalar quantity child, and is shown in 403 of drawing 5 using this property (Zij (i, j=1-4) is obtained.)
[0031] The number of bits of each element of the output matrix (Zij (i, j=1-4)) of the Hadamard transform which were-izing [ the Hadamard transform / number / of each element of the 1-block lightness information Xij (i, j=1-4) ], and was formed into the scalar quantity child by drawing 6 (c) in the number of bits of each element of the output matrix (Yij (i, j=1-4)) of a Hadamard transform is shown in drawing As shown in these drawings, Y11, i.e., a dc component, is quantized to most 8 bits, it is referred to as Z11, and each Yij is quantized with such a few number of bits that spatial frequency is high.
[0032] Furthermore, as 16 elements of Zij (i, j=1-4) are shown in 404 of drawing 5 , grouping is carried out to a dc component and four alternating current components. Namely, as shown in Table 2, Z11 is assigned to AVE as a dc component. As a horizontal-scanning alternating current component, carry out grouping of Z21, Z13, and Z14 to L1, and they are assigned to it. As a vertical-scanning alternating current component, carry out grouping of Z21, Z31, and Z41 to L2, and they are assigned to it. As an inside region alternating current component of horizontal scanning and vertical scanning, grouping of Z22, Z23, Z32, and Z33 is carried out to M, they are assigned to it, as a high region component of horizontal scanning and vertical scanning, grouping of Z24, Z42, Z43, and Z44 is carried out to H, and they are assigned to it.
[0033]
[Table 2]

| | | |
|---|---|---|
| AVE | 直流成分（平均値）相当 | $Z_{11}$ |
| L1 | 主走査直交成分 | $Z_{12}$, $Z_{13}$, $Z_{14}$ |
| L2 | 副走査交流成分 | $Z_{21}$, $Z_{31}$, $Z_{41}$ |
| M | 主副中域交流成分 | $Z_{22}$, $Z_{23}$, $Z_{32}$, $Z_{33}$ |
| H | 主副高域交流成分 | $Z_{24}$, $Z_{34}$, $Z_{42}$, $Z_{43}$, $Z_{44}$ |

In drawing 4 , 701-703 are line memory, it is delaying the image data of one line, respectively, and a pixel block which was shown in drawing 7 is started. 704 is a Hadamard transform circuit and performs conversion shown by (3) formulas.
[0034] Namely, as shown in drawing 8 , it synchronizes with CLK signal and XPHS signal. 704 Hadamard transform circuit X1 **** -- X11, X12, X13, and X14 signal 704 Hadamard transform circuit X2 **** -- X21, X22, X23, and X24 signal -- 704 Hadamard transform circuit X3 **** -- X31, X32, X33, and X34 signal -- 704 Hadamard transform circuit X4 X41, X42, X43, and X44 signal are inputted. Moreover, the signal by which the Hadamard transform was carried out is delayed by CLK signal 8 pulse. Y1 of the Hadamard transform circuit 704 **** -- Y11, Y12,

Y13, and Y14 Y2 of the Hadamard transform circuit 704 **** -- Y21, Y22, Y23, and Y24 -- Y3 of the Hadamard transform circuit 704 **** -- Y31, Y32, Y33, and Y34 -- Y4 of the Hadamard transform circuit 704 **** -- Y41, Y42, Y43, and Y44 are outputted

[0035] 705-708 are ROMs for LUT respectively, and are a fraction which performs scalar quantity child-ization explained by drawing 5 - view 6 . that is, it quantizes to the number of bits which shows the output by which the Hadamard transform was carried out in drawing 6 (c) -- as -- ROMs 705-708 -- beforehand, as the output after the Hadamard transform used as an input, and an output corresponding to XPHS signal, data are written in each address so that the result formed into the scalar quantity child may be outputted 709 is a circuit (henceforth a grouping circuit) which performs grouping for vector quantization, and shows the detailed configuration to drawing 9 - view 10 .

[0036] In drawing 9 - view 10 , 801-816 are flip-flop circuits respectively, the retardation which synchronized with CLK signal is given, the data in 1 block which consists of the 4 pixel x4 line shown in 403 of drawing 5 are held, and the data divided into each group of AVE, L1, L2, M, and H which are shown in 404 and Table 2 of drawing 5 from the inside are extracted. 817-821 are 2->1 selectors respectively, when "0" is inputted into the switch terminal, the value of A side input is outputted to an output terminal (Y), and when "1" is inputted into S, the value of B side input is outputted to an output terminal (Y).

[0037] Moreover, 822-826 are flip-flop circuits, and give the retardation which synchronized with CLK signal. XD0 signal synchronizes with CLK signal and XPHS signal, as shown in drawing 8 . It is the signal which is set to "0" only when XPHS signal is "0", and is set to "1" in except [ it ]. The output of selectors 817-821 is delayed for one pulse of CLK signal with flip-flops 822-826 as a result by the scalar quantity child-ized result for every group which consists of 4 pixel x4 line and which was shown in Table 2 for every block. It is outputted to the timing shown in drawing 8 from Q output of each flip-flop. Furthermore, 827-831 are flip-flop circuits, input data is held in the standup of CLK4 signal, and each signal of AVE, L1, L2, M, and H is outputted to the timing shown in drawing 8 .

[0038] Furthermore in drawing 4 , 710-713 are ROMs for LUT., respectively L1, L2, M of the grouping circuit 709, And it is what quantizes the signal outputted from H with well-known vector quantization technique. The group of 9 bits and L2 for the group of L1, respectively 9 bits, It is outputted as an L-code signal to the timing which 8 bits quantizes the group of 8 bits and H, and a synchronization is taken in the standup of CLK4 signal with a flip-flop 714, and shows the group of M in drawing 8 .

[0039] 715 is LGAIN calculation machine. moreover, to each input terminal of A, B, C, and D Input terminals X1, X2, X3, and X4 of the Hadamard transform circuit 704 To the same timing as an input It is L* at the block unit which consists of 4 pixel x4 line. A signal is inputted. LGAIN signal and L* which are the amplitude (maximum-minimum value) of a lightness signal (L*) about each block The positional information (coordinate within a block) LMX which takes maximum, and L* The positional information (coordinate within a block) LMN which takes the minimum value is computed.

[0040] Drawing 11 is a block diagram showing the detailed configuration of LGAIN calculation machine 715. In drawing 11 , 901-904 are flip-flops and hold input data in the standup of CLK signal. 905 is the reference circuit of the maximum of the orientation of vertical scanning, and the minimum value, and shows the detailed configuration in drawing 12 .

[0041] As for the selector of 2->1, and 1003, in drawing 12 , 1001-1002 are [ a comparator and 1004 ] inverters. About the data inputted into selectors 1001-1002, A input terminal of a comparator 1003, and B input terminals of each, if it is A(input value to A input terminal) >B (input value to B input terminal) The output of the output terminal (Y) of a comparator 1003 is set to "1", and B signal with which A signal inputted into A input terminal was inputted into B input terminal from the output terminal (Y) of a selector 1002 is outputted from the output terminal (Y) of a selector 1001. On the other hand, if it is A<=B, the output of the output terminal (Y) of a comparator 1003 will be set to "0", and A signal with which B signal inputted into B input terminal was inputted into A input terminal from the output terminal (Y) of a selector 1002 will

be outputted from the output terminal (Y) of a selector 1001. Consequently, from the output terminal (Y) of a comparator 1001, the value of max (A, B) is outputted and the value of min (A, B) is outputted from the output terminal (Y) of a comparator 1002.
[0042] Similarly, as for the selector of 2->1, and 1007, 1005-1006 are [ a comparator and 1008 ] inverters. About the data inputted into selectors 1005-1006, A input terminal of a comparator 1007, and B input terminals of each, if it is C(input value to A input terminal) >D (input value to B input terminal), here The output of the output terminal (Y) of a comparator 1007 is set to "1", and D signal with which C signal inputted into A input terminal was inputted into B input terminal from the output terminal (Y) of a selector 1006 is outputted from the output terminal (Y) of a selector 1005. On the other hand, if it is C<=D, the output of the output terminal (Y) of a comparator 1007 will be set to "0", and C signal with which D signal inputted into B input terminal was inputted into A input terminal from the output terminal (Y) of a selector 1006 will be outputted from the output terminal (Y) of a selector 1005. Consequently, from the output terminal (Y) of a comparator 1005, the value of max (C, D) is outputted and the value of min (C, D) is outputted from the output terminal (Y) of a comparator 1004.
[0043] furthermore, when a comparator, and 1012-1014 are inverters and 2->1 selector and 1010 are max(A, B) >maxes (C, D), 1009 and 1011 The output of a comparator 1010 is set to "1" and the value of max (A, B) is outputted from the output terminal (Y) of a selector 1009, and in being max(A, B) <=max (C, D) The output of a comparator 1010 is set to "0" and the value of max (C, D) is outputted from the output terminal (Y) of a selector 1009. Consequently, the value of max (A, B, C, D) is outputted as a signal (max) from the output terminal (Y) of a selector 1009. Moreover, the code which shows any should take maximum between A, B, C, and D is outputted to the signal imx (0) and the signal imx (1) as follows. That is, it is set to imx(1) =0 and imx(0) =1, when A takes maximum, imx(1) =0 and imx(0) =0, and B take maximum, imx(1) =0 and imx (0) =1, and C take maximum and imx(1) =1 and imx(0) =0, and D take maximum.
[0044] Similarly, when it is a comparator and it is min(A, B) >min (C, D), 1015 and 1017 2->1 selector and 1016 The output of a comparator 1016 is set to "1" and the value of min (C, D) is outputted from the output terminal (Y) of a selector 1015, and in being min(A, B) <=min (C, D) The output of a comparator 1016 is set to "0" and the value of min (A, B) is outputted from the output terminal (Y) of a selector 1015. Consequently, the value of min (A, B, C, D) is outputted as a signal (min) from the output terminal (Y) of a selector 1015. Moreover, the code which shows any should take the minimum value between A, B, C, and D is outputted to the signal imn (0) and the signal imn (1) as follows. That is, it is set to imn(1) =1 and imn(0) =1, when A takes the minimum value, imn(1) =0 and imn(0) =0, and B take the minimum value, imn(1) =0 and imn(0) =1, and C take the minimum value and imn(1) =1 and imn(0) =0, and D take the minimum value.
[0045] Now, again, in drawing 11 , 906-913 are flip-flop circuits respectively, and give the retardation only for one pulse of CLK signal for max, min, imx, and imn which are the output signal of the maximum / minimum value reference circuit 905 of the orientation of vertical scanning, respectively. Moreover, 914 is a circuit which searches the maximum of the orientation of horizontal scanning, and shows the detailed configuration in drawing 13 .
[0046] As for 2->1 selector and 1102, in drawing 13 , 1101 is [ a comparator and 1103 ] inverters. Two input signal terminals A and B are in a selector 1101 and the comparator 1102 respectively, A signal is inputted into a generator terminal and B signal is inputted into a battery terminal. Here, if it is A(value of A signal) >B (value of B signal), the output of a comparator 1102 will be set to "1" and A signal will be outputted to the output terminal (Y) of a selector 1101. On the other hand, if it is A<=B, the output of a comparator 1102 will be set to "0" and B signal will be outputted to the output terminal (Y) of a selector 1101. Consequently, the value of max (A, B) is outputted to the output terminal (Y) of a selector 1101.
[0047] Moreover, in a selector 1104, about two input signals iA and iB to the selector, supposing it is A(value of iA signal) >B (value of iB signal), iA signal will be outputted from the output terminal (Y) of a selector 1104, and if it is A<=B, iB signal will be outputted from the output terminal (Y) of a selector 1104.
[0048] Similarly, as for 2->1 selector and 1106, 1105 is [ a comparator and 1107 ] inverters. Two

input signal terminals A and B are in a selector 1105 and the comparator 1106 respectively, C signal is inputted into a generator terminal and D signal is inputted into a battery terminal. Here, if it is C(value of C signal) >D (value of D signal), the output of a comparator 1106 will be set to "1" and C signal will be outputted to the output terminal (Y) of a selector 1105. On the other hand, if it is C<=D, the output of a comparator 1106 will be set to "0" and D signal will be outputted to the output terminal (Y) of a selector 1105. Consequently, the value of max (C, D) is outputted to the output terminal (Y) of a selector 1105.

[0049] Moreover, in a selector 1108, about two input signals iC and iD to the selector, supposing it is A(value of iC signal) >B (value of iD signal), iC signal will be outputted from the output terminal (Y) of a selector 1108, and if it is A<=B, iD signal will be outputted from the output terminal (Y) of a selector 1108.

[0050] Furthermore, as for 2->1 selector and 1110, 1109, 1111, and 1113 are [ a comparator and 1112 ] inverters. the selector 1109 and the comparator 1110 -- about the input signal to each two input terminals A and B of each, when it is max(A, B) >max (C, D), the output of a comparator 1110 is set to "1" and max (A, B) is outputted to the output terminal (Y) of a selector 1109 On the other hand, when it is max(A, B) <=max (C, D), the output of a comparator 1110 is set to "0" and max (C, D) is outputted to the output terminal (Y) of a selector 1109. Consequently, the value of max (A, B, C, D) is outputted to the output terminal (Y) of a selector 1109.

[0051] Moreover, the value of an output signal imx (0), imx (1), and imx (3-2) is determined as follows by which input takes maximum among input signals A, B, C, and D. Namely, when A takes maximum and imx(3-2) =iA, imx(1) =0, and imx(0) =0B take maximum, It is set to imx(3-2) =iD, imx(1) =1, and imx(0) =1, when imx(3-2) =iB, imx(1) =0, and imx(0) =1C take maximum and imx(3-2) =iC, imx(1) =1, and imx(0) =0D take maximum.

[0052] Thus, imx is L*. A signal turns into the signal which shows the position (coordinate) which is among 1 block which consists of 4 pixel x4 line, and takes maximum.

[0053] On the other hand, in drawing 11 , 915 is a circuit which searches the minimum value of the orientation of horizontal scanning, and shows the detail in drawing 14 .

[0054] In drawing 14 , 1201 is 2->1 selector and 1202 is a comparator. Two input signal terminals A and B are in a selector 1201 and the comparator 1202 respectively, A signal is inputted into a generator terminal and B signal is inputted into a battery terminal. Here, if it is A(value of A signal) >B (value of B signal), the output of a comparator 1202 will be set to "1" and B signal will be outputted to the output terminal (Y) of a selector 1201. On the other hand, if it is A<=B, the output of a comparator 1202 will be set to "0" and A signal will be outputted to Y output of a selector 1201. Consequently, the value of min (A, B) is outputted to the output terminal (Y) of a selector 1201.

[0055] Moreover, about two input terminal A of a selector 1203, and the input signals iA and iB inputted into B of each, supposing it is A(value of iA signal) >B (value of iB signal), iB signal will be outputted from the output terminal (Y) of a selector 1203, and if it is A<=B, iA signal will be outputted from the output terminal (Y).

[0056] Similarly, 1204 is 2->1 selector and 1205 is a comparator. Two input signal terminals A and B are in a selector 1204 and the comparator 1205 respectively, C signal is inputted into a generator terminal and D signal is inputted into a battery terminal. Here, if it is C>D, the output of a comparator 1205 will be set to "1" and D signal will be outputted to the output terminal (Y) of a selector 1204. On the other hand, if it is C<=D, the output of a comparator 1205 will be set to "0" and C signal will be outputted to the output terminal (Y) of a selector 1204. Consequently, the value of min (C, D) is outputted to the output terminal (Y) of a selector 1204.

[0057] Moreover, about two input terminal A of a selector 1206, and the input signals iC and iD inputted into B of each, supposing it is A(value of iC signal) >B (value of iD signal), iD signal will be outputted from the output terminal (Y) of a selector 1206, and if it is A<=B, iC signal will be outputted from the output terminal (Y).

[0058] Furthermore, as for 1207, 1209, and 1210, 2->1 selector and 1208 are comparators. the selector 1207 and the comparator 1208 -- about the input signal to each two input terminals A and B of each, when it is min(A, B) >min (C, D), the output of a comparator 1208 is set to "1" and

min (C, D) is outputted to the output terminal (Y) of a selector 1207 On the other hand, when it is min(A, B) <=min (C, D), the output of a comparator 1208 is set to "0" and min (A, B) is outputted to the output terminal (Y) of a selector 1207. Consequently, the value of min (A, B, C, D) is outputted to the output terminal (Y) of a selector 1207.

[0059] Moreover, the value of an output signal imn (0), imn (1), and imn (3-2) is determined as follows by which input takes the minimum value among input signals A, B, C, and D. Namely, when A takes the minimum value and imn(3-2) =iA, imn(1) =0, and imn(0) =0B take the minimum value, It is set to imn(3-2) =iD, imn(1) =1, and imn(0) =1, when imn(3-2) =iB, imn(1) =0, and imn(0) =1C take the minimum value and imn(3-2) =iC, imn(1) =1, and imn(0) =0D take the minimum value.

[0060] Thus, imn is L*. A signal turns into the signal which shows the position (coordinate) which is among 1 block which consists of 4 pixel x4 line, and takes the minimum value.

[0061] It is L* in 1 block which 916 is a subtractor in drawing 11 and consists of 4 pixel x4 line again. The value which subtracted the minimum value (min) from the maximum (max) of a signal is outputted. As for 917-919, 2->1 selector, and 920-922 are flip-flop circuits. Moreover, as shown in drawing 8 , synchronizing with XPHS signal and CLK signal, XD1 signal is set to "0", only when the value of XPHS signal is "1", and, other than this, is a signal used as "1" then. Furthermore, it is L* at 1 block. LGAIN signal and L* which are the maximum-minimum value of a signal LMX signal and L* which show the position (coordinate) in 1 block in case a signal takes maximum LMN signal which shows the position (coordinate) in 1 block in case a signal takes the minimum value is outputted to the timing shown in drawing 8 .

[0062] 716 of drawing 4 is a comparator, LGAIN signal from LGAIN calculation machine 715 is inputted into input terminal A of a comparator 716, and the signal (a certain constant value) from CPU (un-illustrating) is inputted into the input terminal B. If it becomes A(value of LGAIN signal) >B (signal value from CPU) about the input signal of a comparator 716, the output (LFLG) from a comparator 716 will be set to "1", and it will be set to "0" if it is A<B.

[0063] This LFLG A signal is inputted as a judgment signal of the quantization circuit inside the chromaticity information coding machine 114 mentioned later.

[0064] [Chromaticity component coding machine 114 ( drawing 15 - view 19 )] view 15 is the block diagram showing the configuration of the chromaticity component coding machine 114 of a chromaticity information. And drawing 16 is a timing diagram which shows the timing of the chromaticity component coding machine 114 of operation.

[0065] the line memory which 7201-7203 give retardation of one line in drawing 15 -- it is -- the inside of a chromaticity information, and a* It is for processing a signal in the unit of the block which consists of 4 pixel x4 line. 7204 is a*. It is the quantization circuit of a signal. Moreover, it is the line memory which gives retardation of one line, and 7205-7207 are the inside of a chromaticity information, and b*. It is for processing a signal per block. 7208 is the same b* as 7204. It is the quantization circuit of a signal.

[0066] drawing 17 - view 19 -- a* The signal quantization circuit 7204 and b* It is the block diagram showing the detailed configuration of the signal quantization circuit 7208.

[0067] In drawing 17 - view 18 , 1501-1524 are flip-flop circuits, and are a fraction which gives the retardation which synchronized with the standup of CLK signal, respectively, and performs synchronous doubling with the lightness information coding machine 113. The value which 1525-1526 were 4->1 selectors, and was inputted into the input terminal (A) from the output terminal (Y) when the 2 bit input signal from s input terminal was "0" is outputted. When the 2 bit input signal is "1", output the value inputted into the input terminal (B) from the output terminal (Y), and the value inputted into the input terminal (C) from the output terminal (Y) when the 2 bit input signal was "2" is outputted. When the 2 bit input signal is "3", the value inputted into the input terminal (D) from the output terminal (Y) is outputted. 2 bits of the high orders of LMX signal are inputted into the 2 bit input signal inputted from s input terminal of a selector 1525, and 2 bits of the high orders of LMN signal are inputted into s input terminal of a selector 1526.

[0068] On the other hand, 1531-1542 are flip-flop circuits, and give the retardation which synchronized with the standup of CLK signal, respectively. 1543-1544 are the 4->1 same selectors

as 1525-1526, 2 bits of the low order of LMX signal with which the synchronization was taken are inputted into s input terminal of a selector 1543, and 2 bits of the low order of LMN signal with which the synchronization was taken are similarly inputted into s input terminal of a selector 1544. Thus, it is L* within 1 block. a* in the position (coordinate) whose signal takes maximum A signal (a* signal quantization circuit 7204 ****) or b* The value of a signal is outputted as MX (from b* signal quantization circuit 7208). It is L* within 1 block. a* in the position (coordinate) whose signal takes the minimum value A signal or b* The value of a signal is outputted as MN.
[0069] On the other hand, 1551 is an averaging machine and outputs the average of the input signal inputted from input terminals A, B, C, and D. 1552-1555 are flip-flop circuits, and give the retardation which synchronized with the standup of CLK signal, respectively. 1556 is the same averaging machine as 1551, and outputs the average of the input signal inputted from the input terminals A, B, C, and D. Consequently, a* within 1 block A signal (a* signal quantization circuit 7204 ****) or b* The average of a signal is outputted as ME (from b* signal quantization circuit 7208).
[0070] Furthermore, it is a flip-flop circuit, and 1557-1560 give the retardation which synchronized with the standup of CLK signal, respectively, they take each signal of MX, MN, and ME, and a synchronization, and LGAIN signal is outputted as a LG signal.
[0071] In drawing 19 , as for each signal of MX, MN, ME, and LG, a synchronization is taken in the standup of CLK signal with flip-flops 1601-1604. 1605 being a subtractor and reducing the value of MN from the value of MX -- it is -- the inside of 1 block -- L* The position and L* to which a signal takes maximum a* in the position where a signal takes the minimum value A signal (a* signal quantization circuit 7204 ****) or b* the difference of a signal (to b* signal quantization circuit 7208) -- a value is computed
[0072] furthermore, the difference which 1606, 1610,-1611 are flip-flops, and was computed by the subtractor 1605 -- a value should pass a flip-flop 1606 -- it is inputted into the address (A15-A8) of ROM for LUT1607 On the other hand, LG signal passes through flip-flops 1604 and 1611, and it is inputted into the address (A7 - A0) of ROM for LUT1607, and is LFLG in the address (A16) of ROM for LUT1607. A signal is inputted. In ROM for LUT1607, it is a* within 1 block. A signal (a* signal quantization circuit 7204 ****) or b* The amplitude of the alternating current component of a signal (to b* signal quantization circuit 7208), L* About the ratio (MX-MN) to the amplitude of the alternating current component of a signal / value of LG, it is LFLG. When a signal is "1", the thing quantized to 4 bits and the thing of "0" sometimes quantized to 2 bits are written in beforehand, and is outputted as data.
[0073] Similarly, in ROM for LUT1618, it is a* in 1 block. A signal (a* signal quantization circuit 7204 ****) or b* About the value of the average ME of a signal (to b* signal quantization circuit 7208), it is LFLG. When a signal is "1", at the thing quantized to 6 bits, and the time of "0", the thing with 8 bits is written in beforehand and outputted as data. The data of ROMs for LUT 1607 and 1618 follow the frequency distribution of the image data obtained experientially. LFLG The output data from ROM for LUT1618 in case a signal is "1" are a* and b* so that the repeatability of the highlight fraction of image data may become good. It is quantizing nonlinear so that the value of a signal may assign many codes to the method of the parvus.
[0074] gain signal and mean signal are outputted to the timing with which 1608 and 1612 are flip-flop circuits and indicated 2->1 selector, and 1609, 1613-1617 to be to drawing 16 .
[0075] [Operation timing [ of equipment ] ( drawing 20 )] view 20 is a timing diagram which shows the timing of the image processing system of this example of operation. In drawing 20 , the signal and WPE signal with which START signal shows manuscript reading operation start of the image processing system of this example are a signal with which an image scanner expresses time to read a manuscript and perform coding processing and memory writing. Moreover, ITOP signal is a signal which shows start of a print operation, MPE signal is a section signal which drives the Magenta semiconductor laser 216 shown in drawing 1 , CPE signal is a section signal which drives the cyano semiconductor laser 215 shown in drawing 1 , YPE signal is a section signal which drives the yellow semiconductor laser 214 shown in drawing 1 , and BPE signal is a section signal which drives the black semiconductor laser 213 shown in drawing 1 .

[0076] it is shown in drawing 20 -- as -- CPE signal, YPE signal, and BPE signal -- respectively -- MPE signal -- receiving -- time intervals t1, t2, and t3 only -- it is delayed These values are respectively controlled to the spacing (d1) with the photoconductor drums 228 and 227 shown in drawing 1 , the spacing (d2) with photoconductor drums 228 and 226, and the spacing (d3) with photoconductor drums 228 and 225 to have a relation called t1 =d1 / v, t2 =d2 / v, and t3 =d3 / v (v is the feed rate of a form).
[0077] HSYNC signal is a horizontal-scanning synchronizing signal, and CLK signal is a pixel synchronizing signal. YPHS signal is the counted value of a 2-bit vertical-scanning counter, and XPHS signal is the counted value of a 2-bit horizontal-scanning counter. These signals are generated by an inverter 1801 and the 2 bit counters 1802 and 1803, as HYSNC signal is considered as an input and START signal is shown in drawing 21 . BLK signal is a periodic signal of a 1 block unit, and processing is made per 1 block to the timing shown by BDATA.
[0078] [Area processing ( drawing 22 - view 23 )] view 22 is the block diagram showing the configuration of area processing circuit 115b which performs area processing per block. In drawing 22 , CLK is a pixel synchronizing signal and HSYNC is a horizontal-scanning synchronizing signal. It is the line memory which gives one line retardation, and 1901-1903 are the output signals X1, X2, and X3 from each line memory. It is delayed by one line, two lines, and three lines in the orientation of vertical scanning to input signal X, respectively. 1904 is X0, X1, X2, and X3 corresponding to [ are an adder and ] the 4 pixels of the orientation of vertical scanning of a binary signal (X). A number is counted although the value is "1" in inside.
[0079] As for 2->1 selector and 1911, 1910 is [ the NOR gate and 1912 ] flip-flops. C1 pixel whose value of the binary signal (X) counted per block synchronizing with BLK signal generated by XPHS (0) and XPHS (1) by the NOR gate 1911 is "1" It is computed and is the value C1. Comparison value C2 beforehand set to the register 1913 It is compared in a comparator 1914. Here, it is C1 >C2. The output (Y) of a comparator 1914 becomes a case with "1", and it is C1 <=C2. The output (Y) is set to "0" and outputted to a case to the timing according to BDATA signal shown in drawing 20 .
[0080] A characteristic thing is that the picture image sign (an L-code signal and ab-code signal) obtained by coding and the characteristic feature signal (K1 and K2) extracted by the feature-extraction circuit 115 correspond to the one for one in the block unit which consists of the 4 pixel x4 line shown in drawing 7 here.
[0081] It is enabled to store in the address which extracts a picture image sign and the characteristic feature signal in each block unit, and is computed from the same address of memory, or the same address by this, or to correspond, respectively and to read, when reading.
[0082] Therefore, since it is enabled to perform this by easy processing by storing in the address which image information and the characteristic feature (attribute) information are made to correspond, and is computed from the same address of memory, or the same address when the writing of memory, and communalization and simplification of a read-out control circuit are attained and it performs edit processing of variable power/rotation on memory, system optimization can be performed.
[0083] Drawing 23 is drawing showing the example of concrete area processing about a character pixel detection. For example, suppose that a part of character 2002 drawn on the manuscript 2001 was judged with K1'=1 by the pixel shown by "O" about each pixel of a part of character 2002 as the judgment result of being a character pixel shows each pixel to 2003, and it was judged with K1'=0 by the other pixel. In this case, signal K1 with which a noise (noise) which is shown in 2004 was mitigated, for example to 1 block by setting C 2 = 4 at area processing circuit 115b It can obtain.
[0084] Moreover, signal K2 corresponding to each block by processing also about judgment result K2' of a black pixel detector in 115d of the area processing circuits of the same configuration It can obtain.
[0085] [Lightness component decryption machinesa [ 117 ]-117d ( drawing 24 )] view 24 is the block diagram showing a lightness component decryption machines [ 117a-117d ] configuration. A decryption of a lightness information is L* by carrying out the reverse Hadamard transform of

the decrypted data with the L-code signal read from the image memory 116. A signal is decrypted. A reverse Hadamard transform is an inverse transformation of a Hadamard transform shown by (3) formulas, and is defined by (4) formulas.

[0086]

$$\begin{bmatrix} X_{11} & X_{12} & X_{13} & X_{14} \\ X_{21} & X_{22} & X_{23} & X_{24} \\ X_{31} & X_{32} & X_{33} & X_{34} \\ X_{41} & X_{42} & X_{43} & X_{44} \end{bmatrix} = (1/4) \cdot H \cdot \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \cdot H^T$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{bmatrix} \quad \cdots\cdots\cdots (4)$$

However, it is the Hadamard matrix of 4x4, and H is HT. It is the transposed matrix of H.

[0087] On the other hand, a Hadamard transform and a reverse Hadamard transform are alignment operations, and when expressing the Hadamard transform or reverse Hadamard transform of matrix X as H (X), generally (5) formulas are realized.

[0088] H(x1+x2+--+x3) = H+(X1) H+ (X2) -- +H (Xn) ..... (5)

Using this property, it decomposes into each frequency band which the lightness information coding machine defined, and a reverse Hadamard transform is performed in parallel, respectively.

[0089] It is YH about the data matrix decrypted by the sign of YM and H in the data matrix decrypted by the sign of YL2 and M in the data matrix decrypted by the sign of YL1 and L2 in the data matrix decrypted by the sign of L1 here. (6) formulas are materialized when carrying out.

[0090]

H(YL1+YL2+YM +YH )

= H(YL1)+H(YL2)+H(YM)+H (YH) ..... (6)

2101-2104 are ROMs for LUT, and the value which computed processing of coding and processing of a reverse Hadamard transform beforehand is held. The sign (9 bits) of L1, the sign (9 bits) of L2, the sign (8 bits) of M, and the sign (8 bits) of H are respectively inputted into the lower bit of the address of ROMs for LUT 2101-2104, and XPHS (2 bits) and YPHS (2 bits) are respectively inputted into the high order bit (4 bits) of the address of ROMs for LUT 2101-2104. An input of the above address outputs the value of the reverse Hadamard transform in the position (coordinate) in each block. 2105 is an adder, is a fraction which performs the addition equivalent to (6) formulas, and is a fraction adding the result of the reverse Hadamard transform in each frequency component (L1, L2, M, H). When the addition result (alternating current component within 1 block of L* signal) is obtained, it passes through a flip-flop 2106 and is L*. It outputs as an alternating current component LAC.

[0091] When decrypting collectively, without using this method, it is not realistic, even if LUT of a total (64 gigabytes) of a total of a 34-bit sign and a 36-bit address space with a coordinate position (XPHS, YPHS) of 4 bits is needed and it is going to realize this technically. However, a configuration becomes easy by using the method explained above that what is necessary is just to prepare some ROMs of a maximum of 13-bit address space (8 K bytes). Moreover, correspondence is easy when changing code length.

[0092] It is an adder and 2107 is L*. The alternating current component LAC and L* The average in 1 block AVE of a signal is added, and it is L* after a decryption. A signal is acquired. With a flip-flop 2108, this signal synchronizes and is outputted to the standup of CLK signal.

[0093] [Chromaticity component decryption machinesa [ 118 ]-118d ( drawing 25 )] view 25 is the block diagram showing a lightness component decryption machines [ 118a-118d ] configuration. ab-code read from the image memory 116 It is decomposed into an a-code signal and a b-code signal, and each is further decomposed into again signal, amean signal, and bgain signal and bmean signal as a synchronization is taken in the standup of CLK signal with a flip-flop 2201 and the signal is shown in drawing 15 . Then, it is a* within 1 block with a multiplier

2202. L* to the amplitude of a signal It is lightness information L* to again signal which is the ratio of the amplitude of a signal. The multiplication of the alternating current component (LAC) is carried out, and it is a* to the value with an adder 2204. amean signal which is the dc component of a signal is added, and it is a*. A signal is decrypted. With a flip-flop 2206, in the standup of CLK signal, decrypted a* signal has a synchronization taken and is outputted.
[0094] Similarly, it is b* within 1 block with a multiplier 2203. L* to the amplitude of a signal It is lightness information L* to bgain signal which is the ratio of the amplitude of a signal. It multiplies by the alternating current component (LAC), and is b* with an adder 2205. bmean signal which is the dc component of a signal is added, and it is b*. A signal is decrypted. Decrypted b* With a flip-flop 2207, in the standup of CLK signal, a signal has a synchronization taken and is outputted.
[0095] [Color space conversion machinesa [ 119 ]-119d ( drawing 26 )] view 26 is the block diagram showing a color space conversion machines [ 119a-119d ] configuration. drawing 26 -- setting -- 2301 -- L*, a*, and b* It is the conversion circuit which changes a signal into an RGB code, and conversion is performed by the formula (7).
[0096]

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \beta_{11}' & \beta_{12}' & \beta_{13}' \\ \beta_{21}' & \beta_{22}' & \beta_{23}' \\ \beta_{31}' & \beta_{32}' & \beta_{33}' \end{bmatrix} \begin{bmatrix} X \\ Y \\ Z \end{bmatrix} \quad \cdots\cdots\cdots (7)$$

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} x^{s} \cdot x_0 \\ y^{s} \cdot y_0 \\ z^{s} \cdot z_0 \end{bmatrix} \quad \cdots\cdots\cdots (8)$$

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} \alpha_{11}' & \alpha_{12}' & \alpha_{13}' \\ \alpha_{21}' & \alpha_{22}' & \alpha_{23}' \\ \alpha_{31}' & \alpha_{32}' & \alpha_{33}' \end{bmatrix} \begin{bmatrix} L^{*} - \alpha_{14} \\ a^{*} - \alpha_{24} \\ b^{*} - \alpha_{34} \end{bmatrix} \quad \cdots\cdots\cdots (9)$$

It corrects.

Moreover, it is the inverse matrix of [alphaij] i of a formula (1), j= 1, and 2 and 3, and [alphaij'] i, j= 1, and 2 and 3 are [betaij'] i, j= 1, and 2 and 3. [betaij] i of a formula (2), j= 1, and 2 and 3 It is an inverse matrix.
[0097] In brightness / concentration converters 2302-2304, conversion according to a formula (10) is performed respectively.
[0098]

$$\left.\begin{array}{l} M_1 = -\log_{10} G \\ C_1 = -\log_{10} R \\ Y_1 = -\log_{10} B \end{array}\right] \quad \cdots\cdots\cdots (10)$$

In the black extraction circuit 2305, conversion according to a formula (11) is performed and a black signal (Bk1) is generated.
[0099]
Bk1 =min (M1, C1, and Y1) ..... (11)
With multipliers 2306-2309, it is C1, M1, Y1, and Bk1 respectively. Coefficients a1, a2, a3, and a4 predetermined to each signal It takes advantaging and an addition operation is performed in an adder 2310. Thus, the **** operation shown in a formula (12) is performed.
[0100] (Outputs C, M, and YorBk) =a1 M1+a2 C1+a3 Y1+a4 Bk1 ..... (12)
To registers 2311-2315, respectively in the case of color space conversion machine 119a a11, a12, a31, and a 41 and 0 in the case of color space conversion machine 119b For a12, a22, a32, and a 42 and 0, in the case of color space conversion machine 119c, a13, a23, a33, and a 43 and 0 are a14, a24, a34, a44, and a'14 in the case of 119d of color space conversion machines. It is set.
[0101] As for a gate circuit and 2330, 2331-2333 are [ a 2 ->1 selector circuit and 2320 ] NAND gate circuits. as a result by the AND of a black pixel judging signal (K1) and a character area judging signal (K2) As a judgment of whether the concerned pixel is a black character area shows

to drawing 27 , it is a1, a2, a3, and a4. A value is chosen, when it is not a black character area, processing according to a formula (13) is performed, and when it is a black character area, processing according to a formula (14) is performed.

[0102]

$$\begin{bmatrix} M \\ C \\ Y \\ Bk \end{bmatrix} = \begin{bmatrix} a_{11} & a_{21} & a_{31} & a_{41} \\ a_{12} & a_{22} & a_{32} & a_{42} \\ a_{13} & a_{23} & a_{33} & a_{43} \\ a_{14} & a_{24} & a_{34} & a_{44} \end{bmatrix} \begin{bmatrix} M_1 \\ C_1 \\ Y_1 \\ Bk_1 \end{bmatrix} \quad \cdots\cdots\cdots (13)$$

$$\begin{bmatrix} M \\ C \\ Y \\ Bk \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ a_{14}' & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} M_1 \\ C_1 \\ Y_1 \\ Bk_1 \end{bmatrix} \quad \cdots\cdots\cdots (14)$$

That is, in a black character area, the output without a color gap can be obtained with outputting in black (Bk) monochrome, as shown in a formula (14). It is based on the RGB code read from CCD sensor by the operation of a formula (13) although it will output by four colors of M, C, Y, and Bk on the other hand except a black character area as shown in a formula (13), and is M1, C1, Y1, and Bk1. A signal is rectified and outputted to M, C, Y, and Bk signal based on the spectral-distribution property of a toner.

[0103] Therefore, if this example is followed, the inputted full color picture signal will be divided into the block unit which consists of 4 pixel x4 line, and it will dissociate and encode in the blocked picture signal unit at a lightness information and a chromaticity information. Especially, according to the amplitude value of the alternating current component of a lightness information, coding of a chromaticity information can change the coding length, and can perform coding.

[0104] In addition, 1 block L* which consists of this example as a judgment signal for separating a picture image area at 4 pixel x4 line Although the difference of maximum and the minimum value was used, this invention is not limited to this. For example, as shown in drawing 28 , the distance on the color space of the maximum of a chromaticity information and the minimum value can also be used.

[0105] namely, inputted a* the signal of every one line is delayed by the line memory 2501-2503 (b* signal is the line memory 2508-2510) -- making -- aGAIN calculation machine 2504 and bGAIN calculation machine 2511 -- it inputs into each input terminals A-D Respectively, the square of aGAIN signal and bGAIN signal which were acquired is carried out by multipliers 2505 and 2512, they are further added by the adder 2506, and are outputted as a rGAIN signal. The threshold by which the rGAIN signal is sent to another input terminal (A) from CPU (un-illustrating) at the input terminal (B) of a comparator 2507 is inputted. Here, if it is A(threshold from CPU) <B (value of rGAIN signal), the output (LFLG) of a comparator 2507 will be set to "1", and, in the case of A>=B, "0" will be outputted.

[0106] Moreover, although this example explained the case where the inputted RGB code was changed into YMCBk signal, this invention is not limited to this. For example, the full color picture signal whose color was separated into red (R), green (G), and blue (B) is also convertible for YUV signal in a conversion circuit 2601 according to a formula (15) like the coding machine of the full color picture image shown in drawing 29 .

[0107]

$$\left.\begin{array}{l} Y = c_1 R + c_2 G + c_3 B \\ U = c_4 (R - Y) \\ V = c_5 (B - Y) \end{array}\right] \quad \cdots\cdots\cdots (15)$$

However, c1, c2, c3, c4, and c5 It is a constant.

[0108] Here, Y is L*. It is the signal with which a lightness information is expressed similarly, and U and V are a*. And b* It is the signal with which a chromaticity is expressed similarly. 2602 is a DCT circuit which performs dispersed cosine conversion, and performs dispersed cosine

conversion (DCT) of an nxn (n is power;n=4 of 2, 8 and 16, and 32 --) pixel. The DCT conversion, it is developed by each spatial-frequency component and a Y signal is encoded by for example, the ******** code with the coding vessel 2606. Furthermore, the amplitude (Y-GAIN) of the Y signal in nx n pixels is computed by the amplitude detector 2603 of Y which has the same configuration as 715. On the other hand, 2604 is a circuit which has the same configuration as 7204, outputs the gain (Ugain) of U signal to the amplitude of a Y signal, and the dc component (Umean) of U signal, unites, and is taken as U-code. Similarly, it is the circuit which has the same configuration as 7204, the gain (Vgain) of V signal to the amplitude of a Y signal and the dc component (Vmean) of V signal are outputted, it doubles, and 2605 is set to V-code. Furthermore, Y-code, U-code, and V-code are put together and it becomes the sign of image data.
[0109] In addition, this invention may be applied to the system which consists of two or more devices, and may be applied to the equipment which consists of one device. Moreover, this invention cannot be overemphasized by that it can apply when attained by supplying a program to a system or equipment.
[0110]
[Effect of the Invention] the full color picture signal which was inputted according to [ as explained above ] this invention is divided into a predetermined unit, and it is alike for every predetermined unit of the, it separates into a lightness information and chromaticity information, and there are coding and an effect that coding few [ of a quality-of-image degradation ] can be performed if it is coding more good [ of luminous efficacy ], i.e., the same quality-of-image degradation, and it is coding short [ of code length ] and the same code length, since especially the dc component of a chromaticity
[0111] By this, since the regeneration picture image after a coding decryption of an input picture image, for example, a half-tone-dot picture image area's, can cancel an azalea, picture image repeatability also improves.

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[Translation done.]

* NOTICES *



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3.In the drawings, any words are not translated.

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of the image processing system which is the typical example of this invention.
[Drawing 2] It is the block diagram showing the configuration of the image-processing circuit 212.
[Drawing 3] It is the block diagram showing the configuration of the image-processing circuit 212.
[Drawing 4] It is the block diagram showing the configuration of the lightness information coding machine 113.
[Drawing 5] It is drawing showing the schema of quantization processing of the blocking picture signal which the lightness information coding machine 113 performs.
[Drawing 6] It is drawing showing the example of quantization processing shown in drawing 4 .
[Drawing 7] It is drawing showing a mode that a picture signal is blocked about the orientation of horizontal scanning, and the orientation of vertical scanning.
[Drawing 8] It is the timing diagram which shows the timing of the lightness information coding machine 113 of operation.
[Drawing 9] It is the block diagram showing the configuration of the grouping circuit 709.
[Drawing 10] It is the block diagram showing the configuration of the grouping circuit 709.
[Drawing 11] It is the block diagram showing the configuration of LGAIN calculation machine 715.
[Drawing 12] It is the block diagram showing the configuration of the maximum / minimum value reference circuit 905 of the orientation of vertical scanning.
[Drawing 13] It is the block diagram showing the configuration of the maximum reference circuit 914 of the orientation of horizontal scanning.
[Drawing 14] It is the block diagram showing the configuration of the minimum value reference circuit 915 of the orientation of horizontal scanning.
[Drawing 15] It is the block diagram showing the configuration of the chromaticity component coding machine 114.
[Drawing 16] It is the timing diagram which shows the timing of the chromaticity component coding machine 114 of operation.
[Drawing 17] a* The signal quantization circuit 7204 and b* It is the block diagram showing the configuration of the signal quantization circuit 7208.
[Drawing 18] a* The signal quantization circuit 7204 and b* It is the block diagram showing the configuration of the signal quantization circuit 7208.
[Drawing 19] a* The signal quantization circuit 7204 and b* It is the block diagram showing the configuration of the signal quantization circuit 7208.
[Drawing 20] It is the timing diagram which shows the timing of the whole image processing system of operation.
[Drawing 21] It is the block diagram showing the configuration of the occurrence circuit of XPHS signal and YPHS signal.
[Drawing 22] It is the block diagram showing the configuration of area processing circuit 115b which performs area processing in the block unit which consists of 4 pixel x4 line.

[Drawing 23] It is drawing showing the example of area processing about a character pixel detection.
[Drawing 24] It is the block diagram showing a lightness component decryption machines [ 117a-117d ] configuration.
[Drawing 25] It is the block diagram showing a chromaticity information decryption machines [ 118a-118d ] configuration.
[Drawing 26] It is the block diagram showing a color space conversion machines [ 119a-119d ] configuration.
[Drawing 27] C1, M1, Y1, and Bk1 which are used for the multiply operation in multipliers 2306-2309 It is drawing showing the value of the coefficient (a1, a2, a3, and a4) to each signal.
[Drawing 28] It is the block diagram showing another example of the judgment signal generation circuit for a separation of a picture image area.
[Drawing 29] It is the block diagram showing another example of the coding machine of a full color picture image.
[Description of Notations]
101~103 CCD
107-109 A/D converter
110-111 Delay circuit
112 Color Space Conversion Machine
113 Lightness Information Coding Machine
114 Chromaticity Information Coding Machine
116 Image Memory
117a-117d Lightness information decryption machine
118a-118d Chromaticity information decryption machine
141-144 Decryption machine
151-156 Tri-state gate
157-160 Variable power circuit
202 Reading Manuscript
212 Image-Processing Circuit
225-228 Photoconductor drum

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[Translation done.]

* NOTICES *



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## CLAIMS

[Claim(s)]
[Claim 1] The input process which is the image-processing technique of processing a full color picture signal, and inputs a full color picture signal, The split process which divides into a predetermined unit the full color picture signal which carried out [ above-mentioned ] the input, The separation process which divides the above-mentioned full color picture signal into a lightness information and a chromaticity information, The lightness information on the above-mentioned full color picture signal is divided into a dc component and an alternating current component for every above-mentioned predetermined unit. A quantization and the quantization process to encode, The 1st calculation process which computes the amplitude of the alternating current component of the above-mentioned lightness information in the above-mentioned predetermined unit, The 2nd calculation process which computes the amplitude of the alternating current component of the above-mentioned chromaticity information in the above-mentioned predetermined unit, The image-processing technique characterized by having the 1st coding process which computes the ratio of the amplitude of the alternating current component of the above-mentioned lightness information to the amplitude of the alternating current component of the above-mentioned chromaticity information, and is encoded, and the 2nd coding process which encodes the dc component of the above-mentioned chromaticity information nonlinear.
[Claim 2] The image-processing technique according to claim 1 characterized by assigning many amounts of sign codes, expressing them as nonlinear coding of the dc component of the above-mentioned chromaticity information to the picture signal with a low chromaticity, and expressing with the few number of codes to the picture signal with a high chromaticity.
[Claim 3] An input means to be the image processing system which processes a full color picture signal, and to input a full color picture signal, A split means to divide into a predetermined unit the full color picture signal which carried out [ above-mentioned ] the input, A separation means to divide the above-mentioned full color picture signal into a lightness information and a chromaticity information, The lightness information on the above-mentioned full color picture signal is divided into a dc component and an alternating current component for every above-mentioned predetermined unit. A quantization and the quantization means to encode, A 1st calculation means to compute the amplitude of the alternating current component of the above-mentioned lightness information in the above-mentioned predetermined unit, A 2nd calculation means to compute the amplitude of the alternating current component of the above-mentioned chromaticity information in the above-mentioned predetermined unit, The image processing system characterized by having a 1st coding means to compute the ratio of the amplitude of the alternating current component of the above-mentioned lightness information to the amplitude of the alternating current component of the above-mentioned chromaticity information, and to encode, and a 2nd coding means to encode the dc component of the above-mentioned chromaticity information nonlinear.
[Claim 4] The image processing system according to claim 3 characterized by assigning many amounts of sign codes, expressing them as nonlinear coding of the dc component of the above-mentioned chromaticity information to the picture signal with a low chromaticity, and expressing with the few number of codes to the picture signal with a high chromaticity.

[Claim 5] The image processing system according to claim 3 characterized by having further an orthogonal transformation means to give orthogonal transformation to a full color picture signal for every above-mentioned predetermined unit.
[Claim 6] The above-mentioned orthogonal transformation is an image processing system according to claim 5 characterized by being a Hadamard transform.
[Claim 7] The above-mentioned orthogonal transformation is an image processing system according to claim 5 characterized by being a discrete Fourier transform or dispersed cosine conversion.
[Claim 8] The code length by which coding was carried out [ above-mentioned ] is an image processing system according to claim 3 characterized by being a fixed-length sign.
[Claim 9] The above-mentioned input means is an image processing system according to claim 3 characterized by having a picture image reading means to read a full color picture image optically and to change into an electrical signal.
[Claim 10] The image processing system according to claim 3 characterized by having further a storage means to store the information on the full color picture image by which coding was carried out [ above-mentioned ].
[Claim 11] The image processing system according to claim 3 characterized by having further a picture image formation means to decrypt the information on the full color picture image by which coding was carried out [ above-mentioned ], and to visualize and output the full color picture image by which the decryption was carried out [ above-mentioned ] to a record medium.
[Claim 12] The above-mentioned picture image formation means is an image processing system according to claim 11 characterized by having a conveyance means to convey a record medium one by one among two or more picture image formation sections corresponding to the color component, and two or more above-mentioned picture image formation sections.

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[Translation done.]

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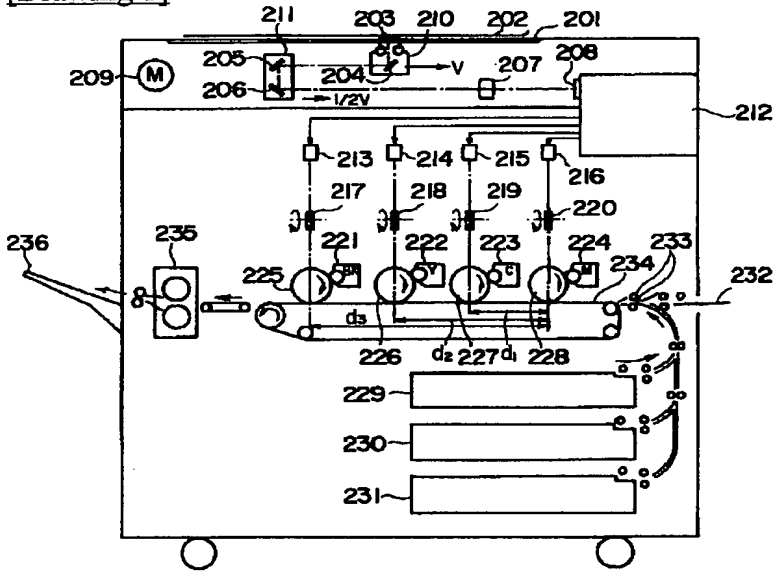
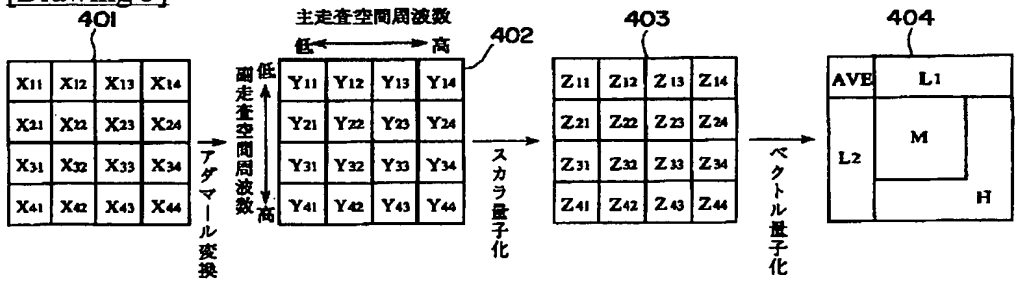
## DRAWINGS

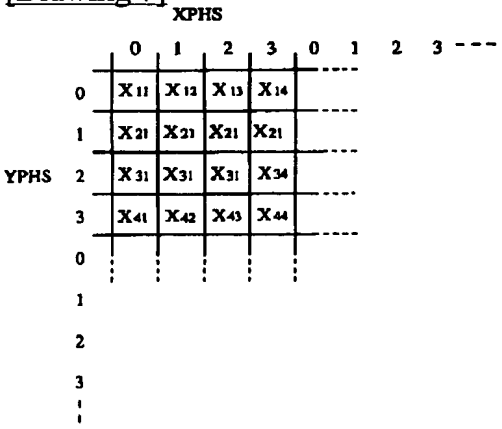
[Drawing 1]



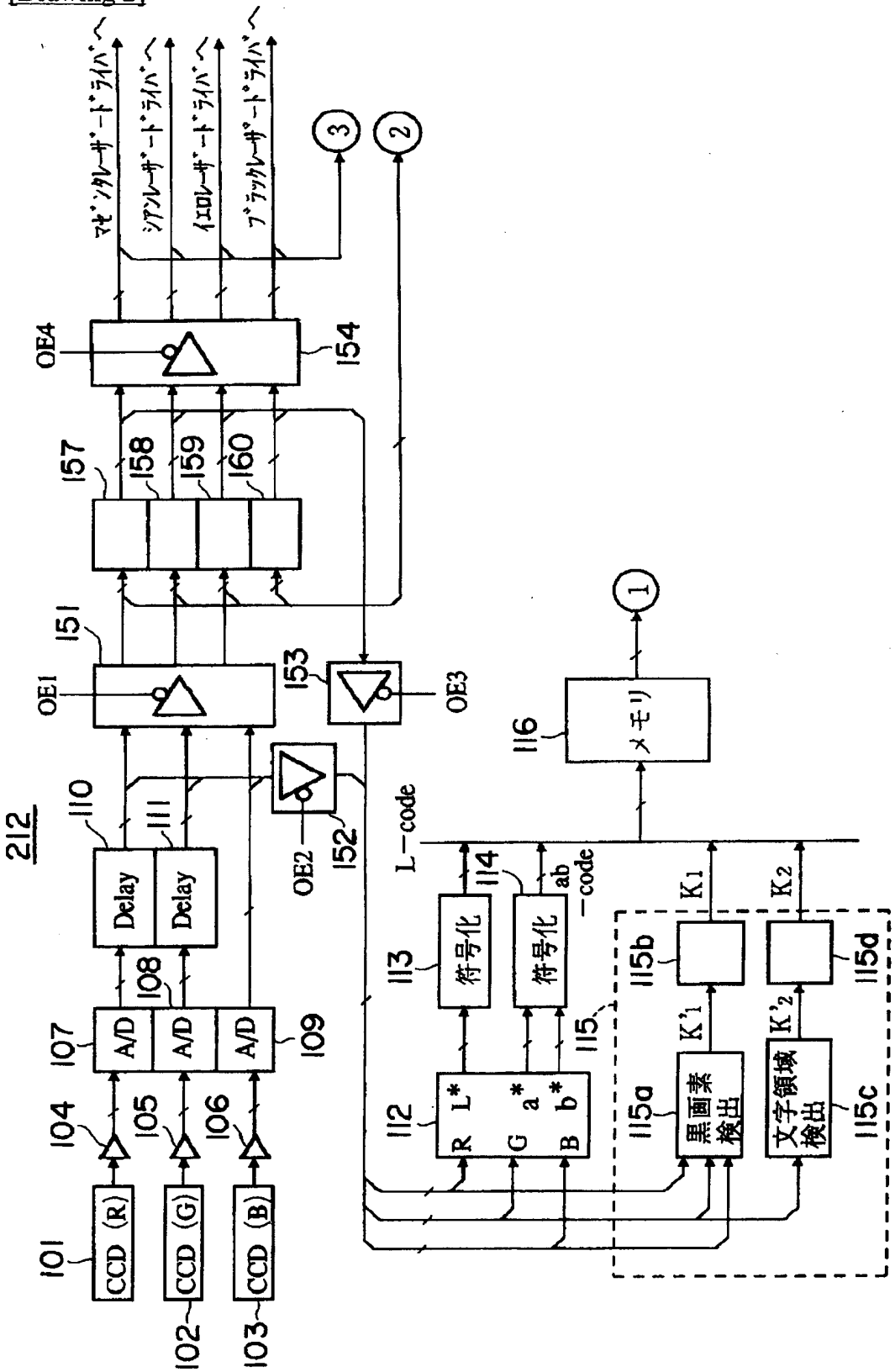

[Drawing 5]



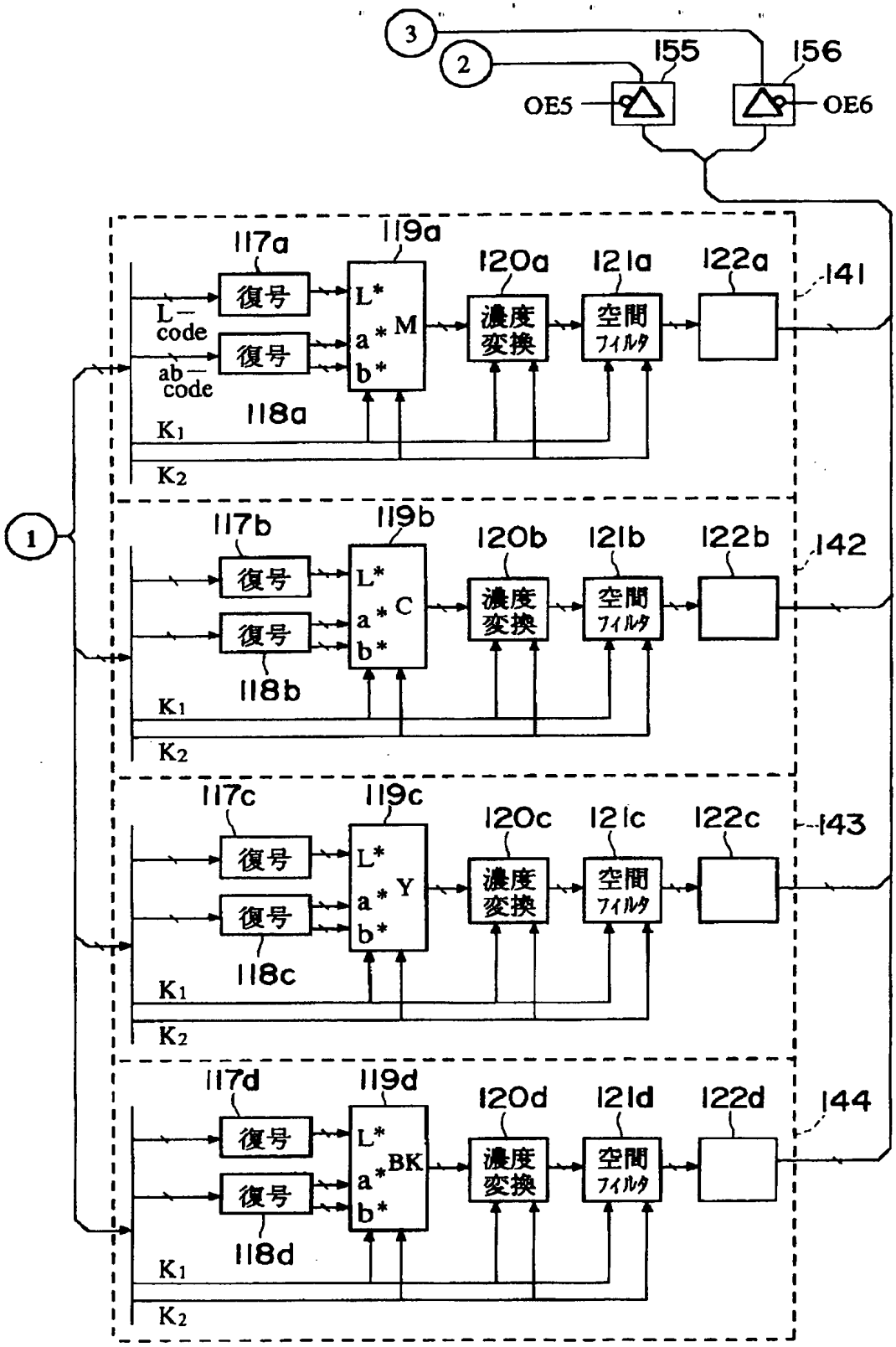

[Drawing 7]



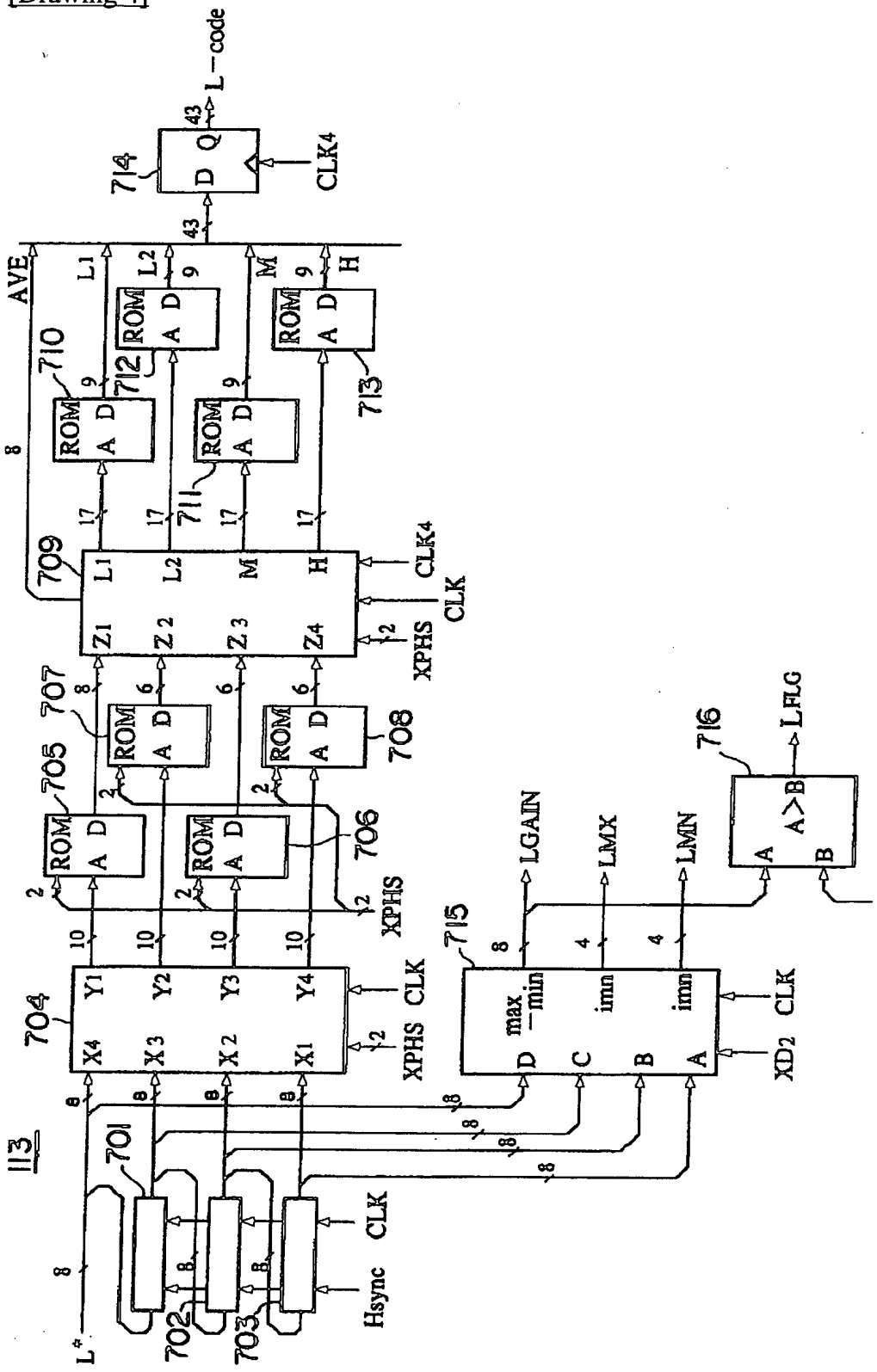
[Drawing 2]




[Drawing 3]


3
2
155
156
OE5
OE6
117a
119a
120a
121a
122a
141
復号
L*
a*
b*
M
濃度変換
空間フィルタ
L−code
ab−code
118a
K1
K2
1
117b
119b
120b
121b
122b
142
C
118b
117c
119c
120c
121c
122c
143
Y
118c
117d
119d
120d
121d
122d
144
BK
118d

[Drawing 4]


L-code
714
CLK4
AVE
710
712
713
711
709
707
708
705
706
704
715
716
LGAIN
LMX
LMN
LFLG
XPHS
CLK
113
701
702
703
Hsync
XD2

[Drawing 6]

| | | | |
|---|---|---|---|
| 8 | 8 | 8 | 8 |
| 8 | 8 | 8 | 8 |
| 8 | 8 | 8 | 8 |
| 8 | 8 | 8 | 8 |

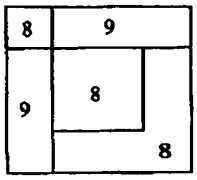
(a)

| | | | |
|---|---|---|---|
| 10 | 10 | 10 | 10 |
| 10 | 10 | 10 | 10 |
| 10 | 10 | 10 | 10 |
| 10 | 10 | 10 | 10 |

(b)

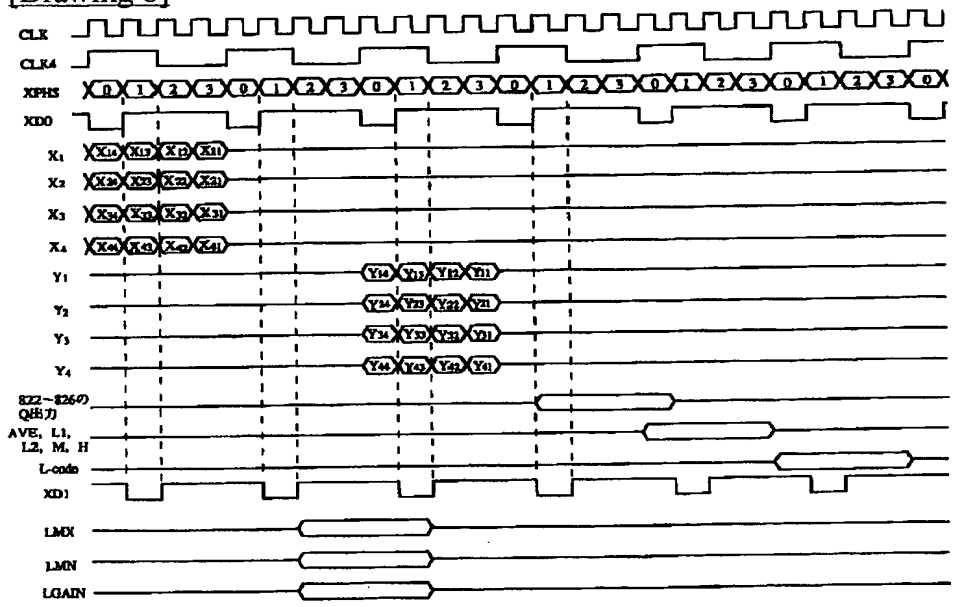
| | | | |
|---|---|---|---|
| 8 | 6 | 6 | 5 |
| 6 | 5 | 4 | 4 |
| 6 | 4 | 4 | 3 |
| 5 | 4 | 3 | 3 |

(c)

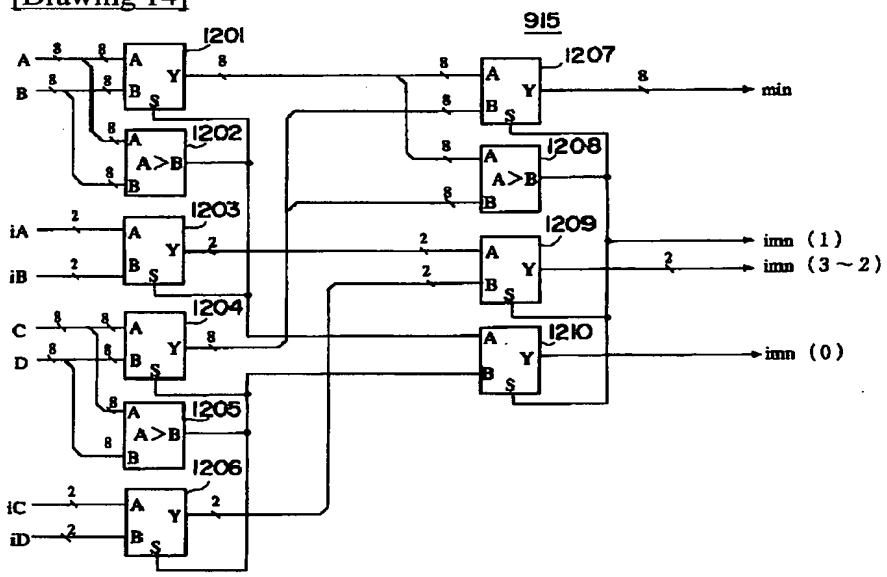



(d)

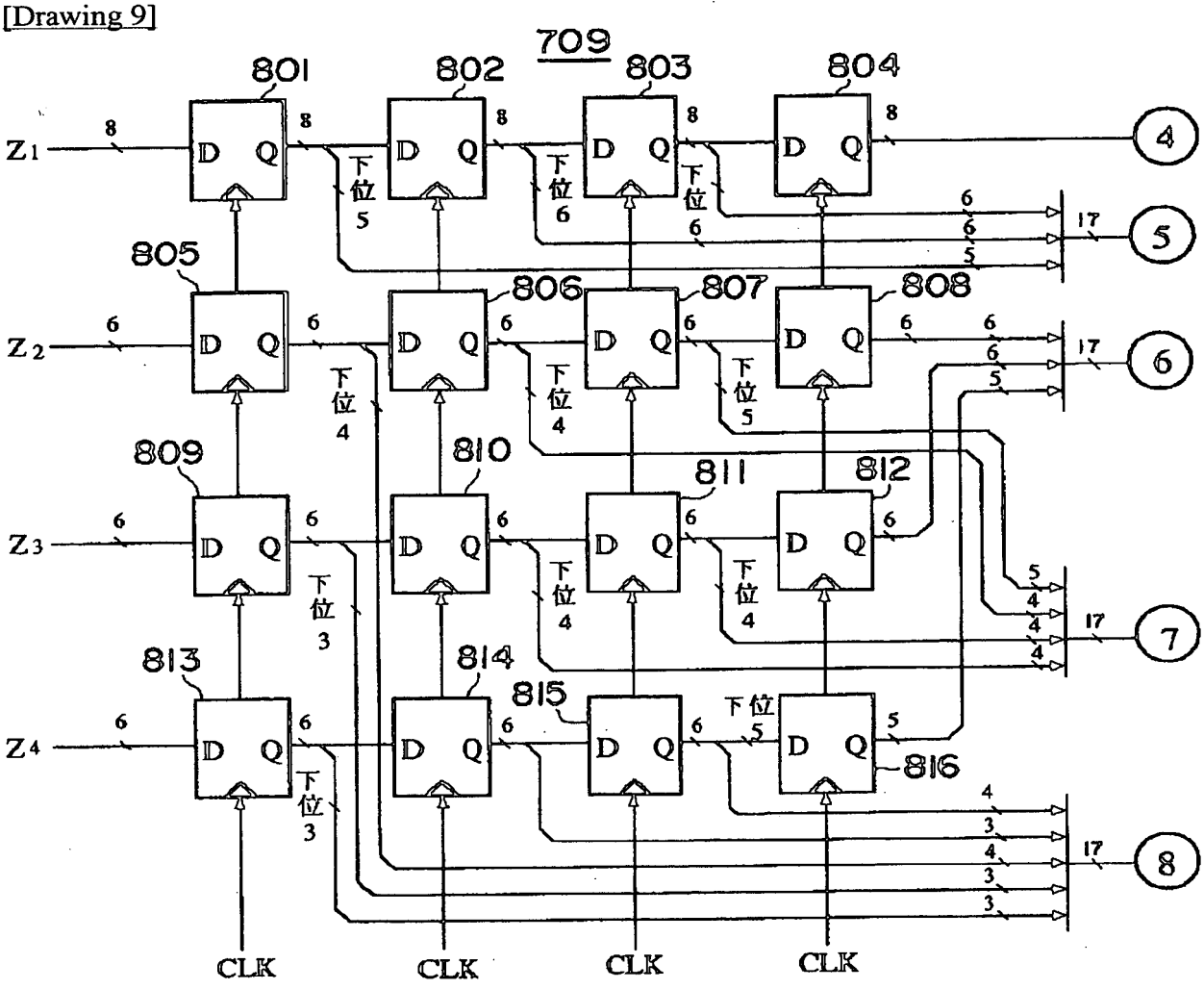
[Drawing 8]



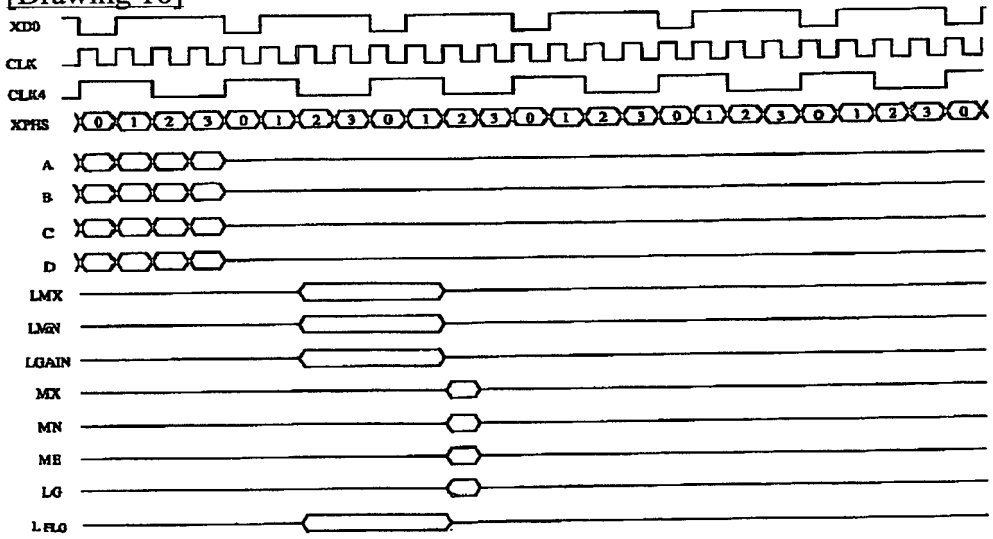

[Drawing 14]



[Drawing 9]

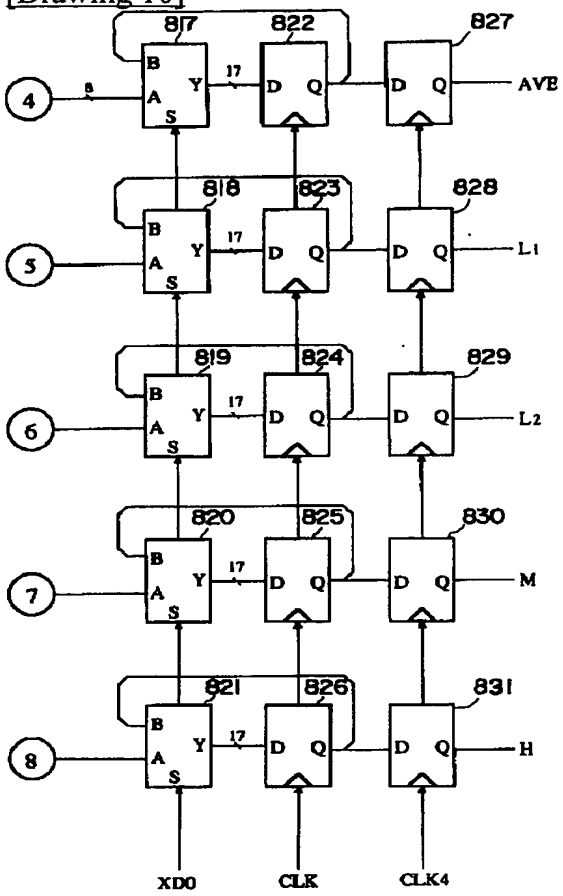



[Drawing 16]

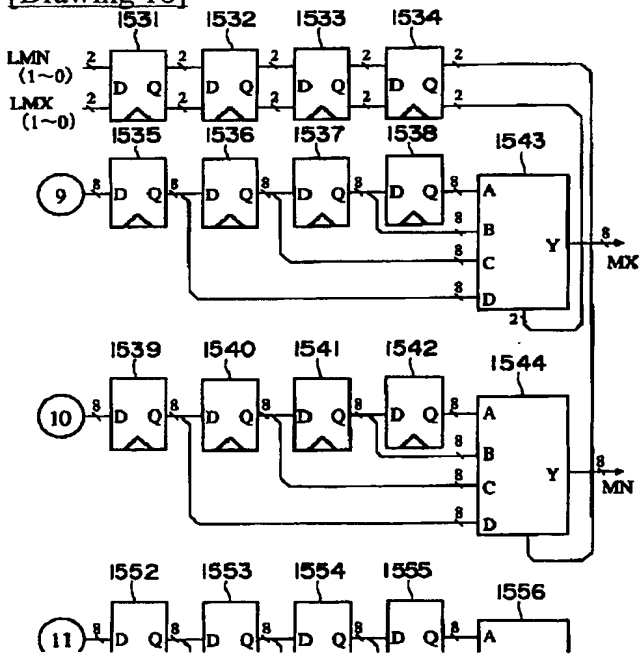


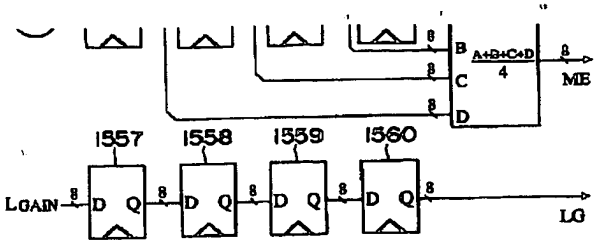
ab-code

[Drawing 10]

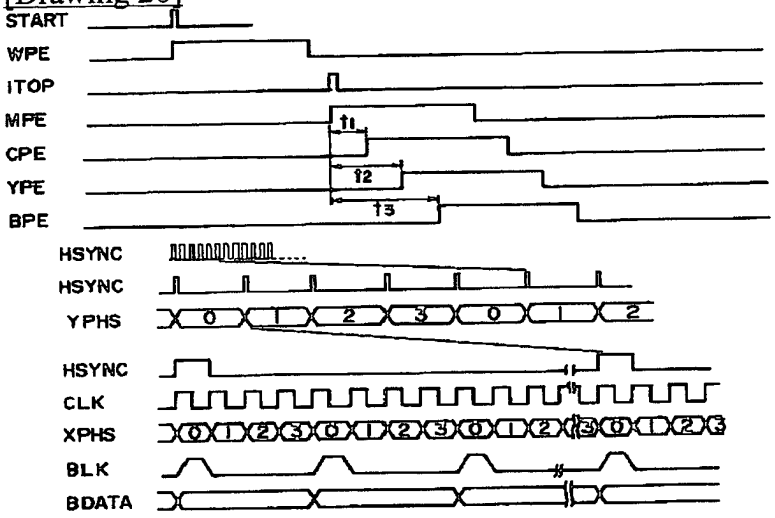



[Drawing 18]

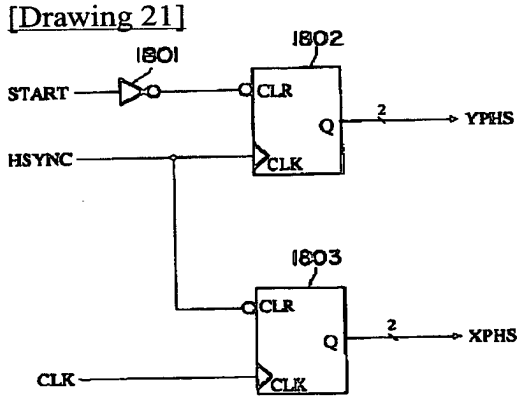




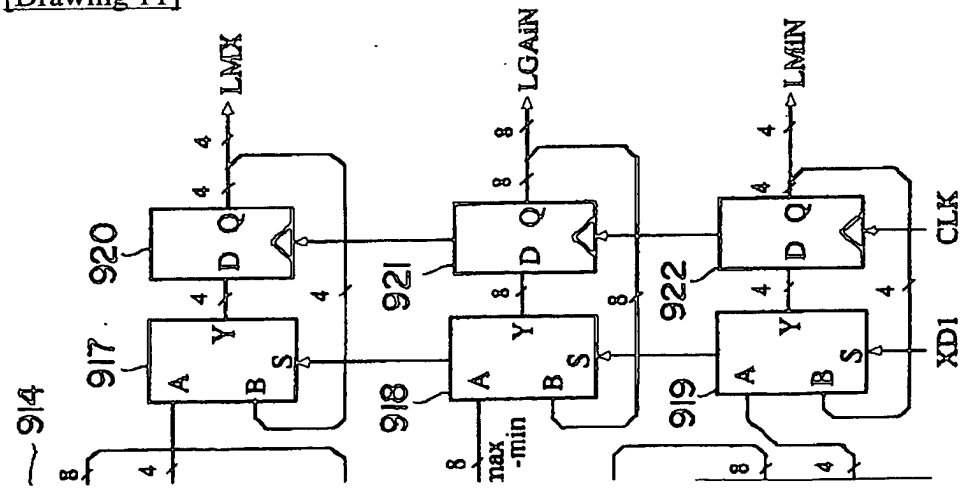

[Drawing 20]

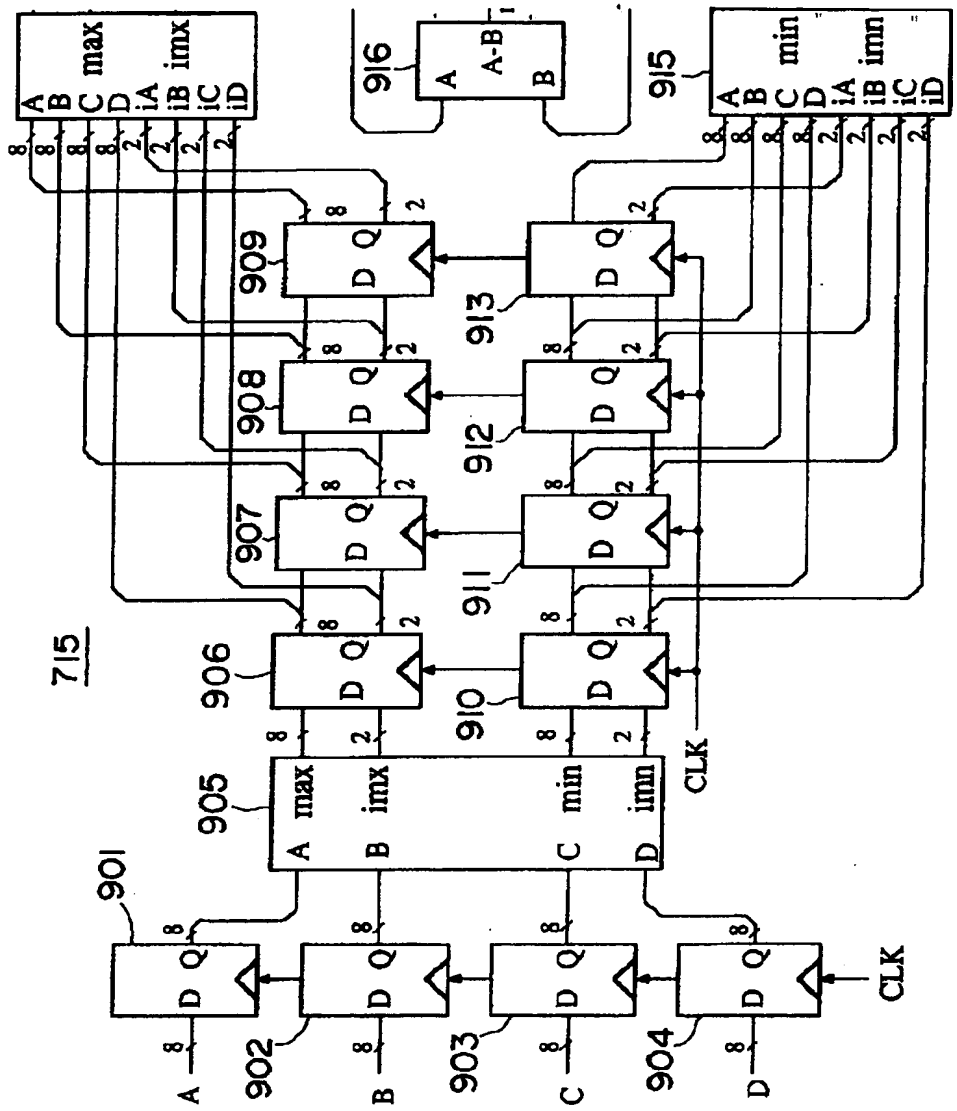



[Drawing 21]

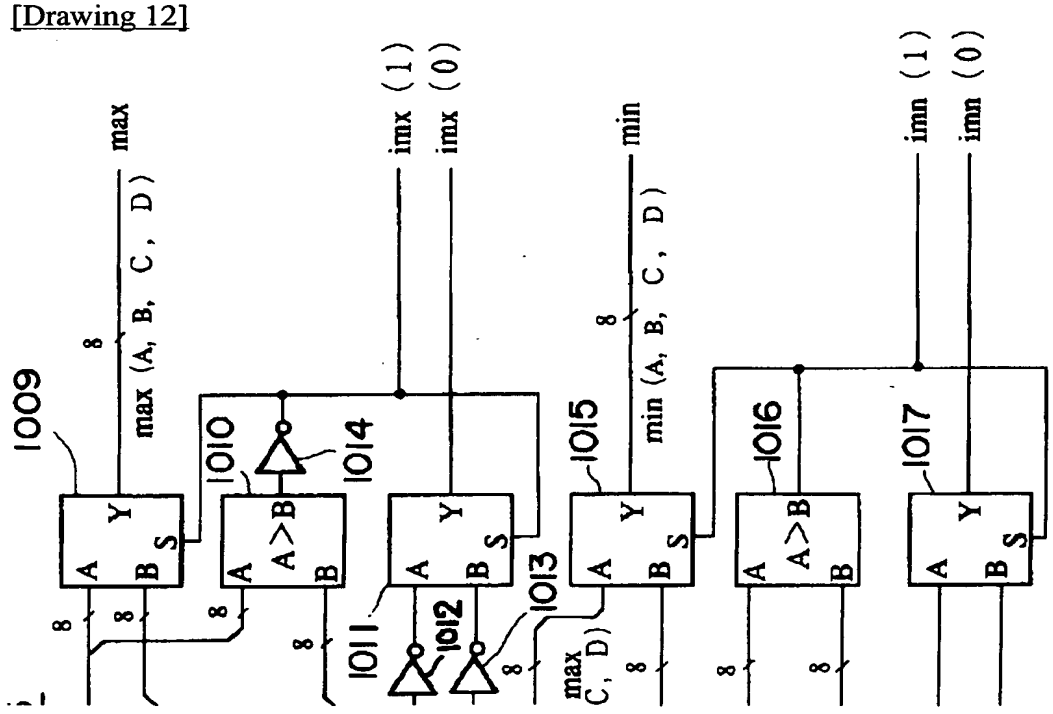


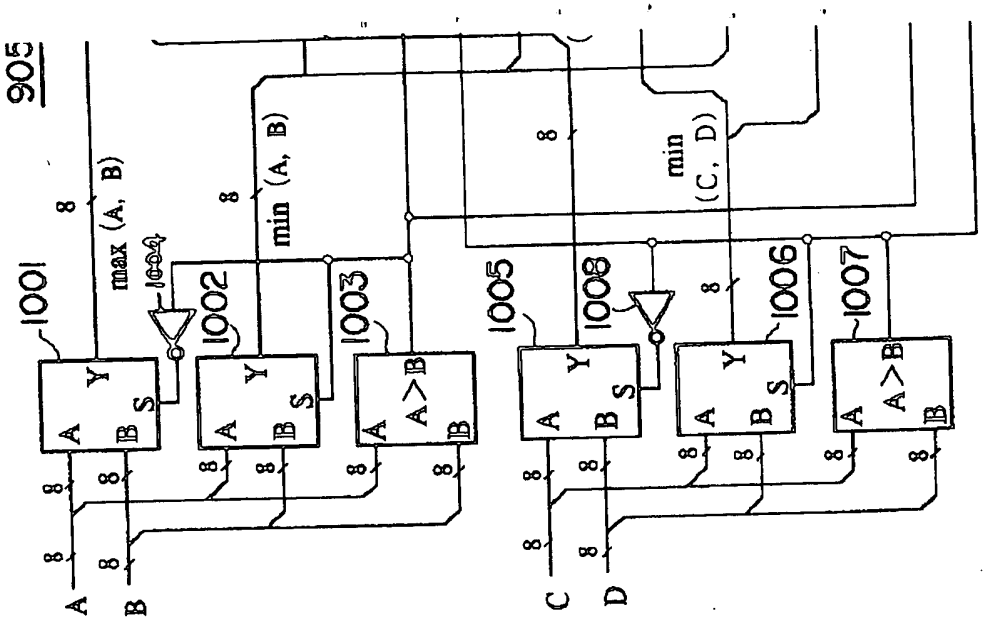

[Drawing 11]



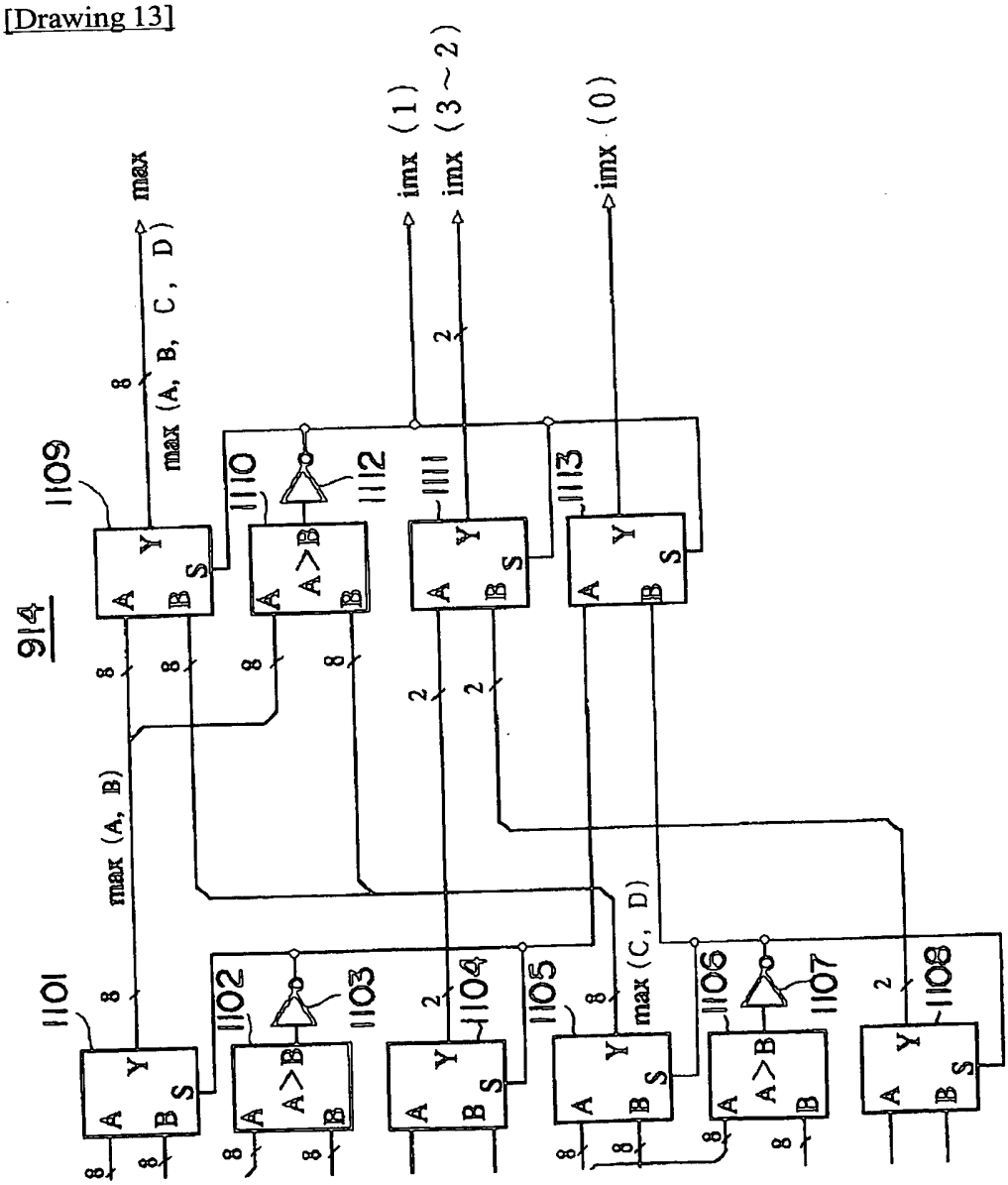

715
901
902
903
904
905
906
907
908
909
910
911
912
913
915
916
A
B
C
D
max
imx
min
imn
CLK
A-B

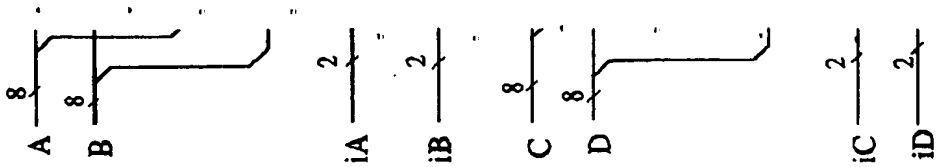
[Drawing 12]


1009
1010
1011
1012
1013
1014
1015
1016
1017
max
max (A, B, C, D)
imx (1)
imx (0)
min
min (A, B, C, D)
imn (1)
imn (0)
A>B
max (C, D)

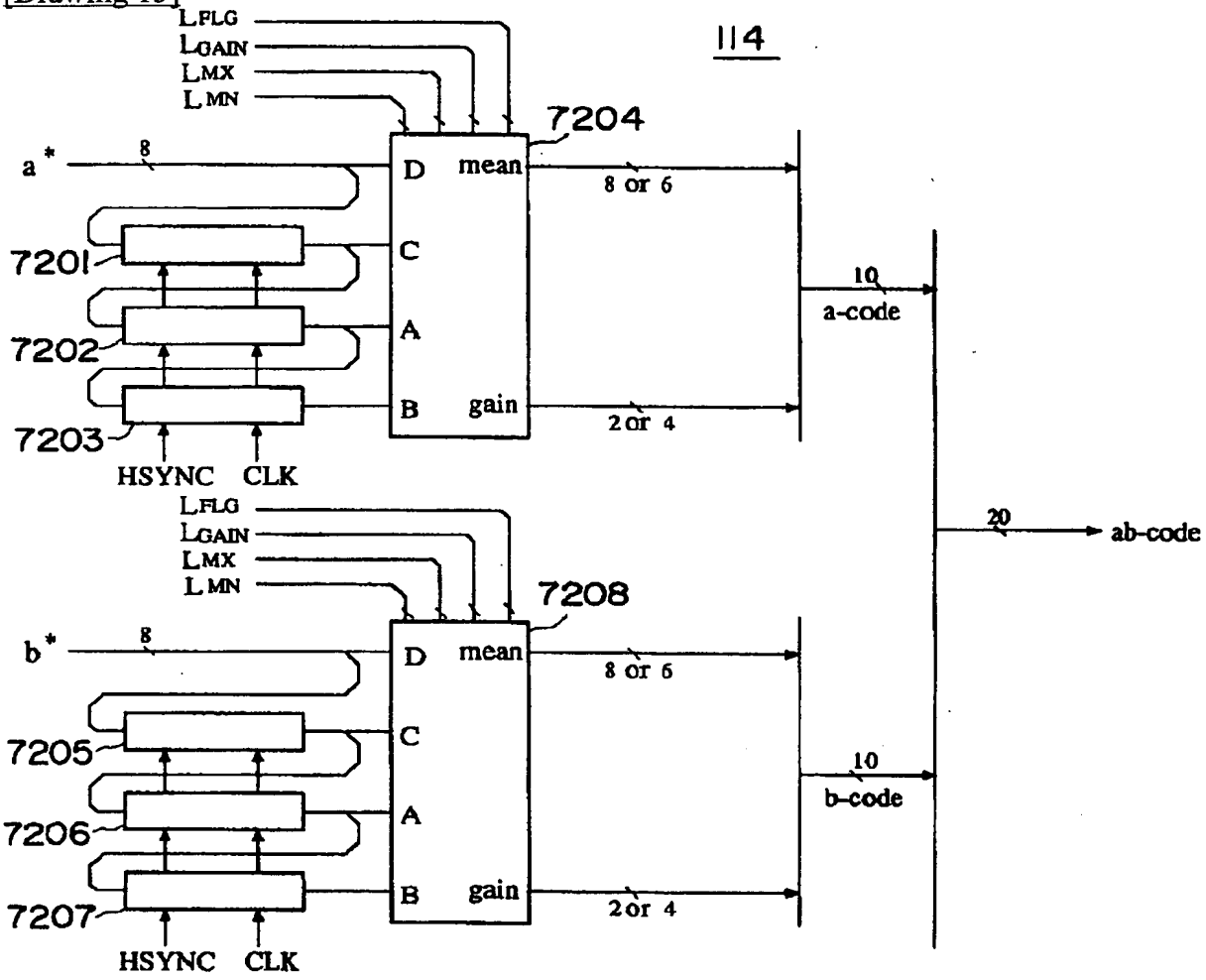

905
1001
1002
1003
1005
1008
1006
1007
max (A, B)
min (A, B)
min (C, D)
A
B
C
D

[Drawing 13]

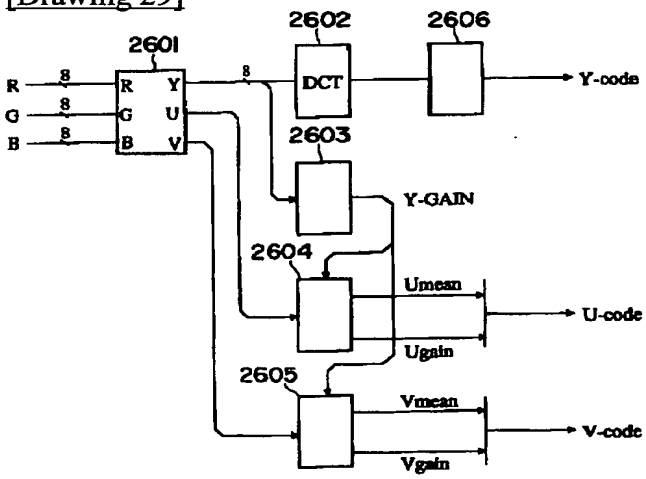

914
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
max
max (A, B, C, D)
imx (1)
imx (3~2)
imx (0)
max (A, B)
max (C, D)



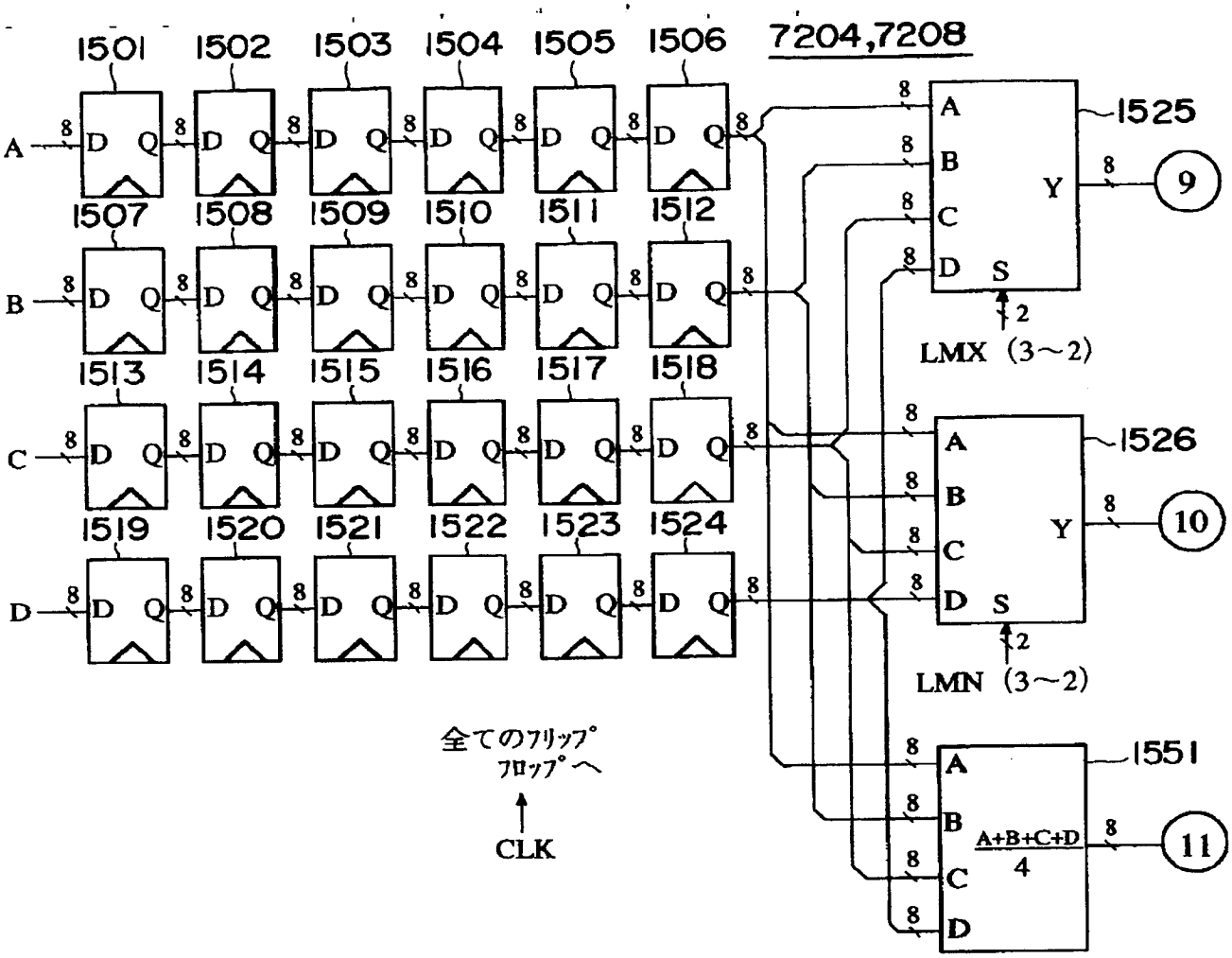

[Drawing 15]



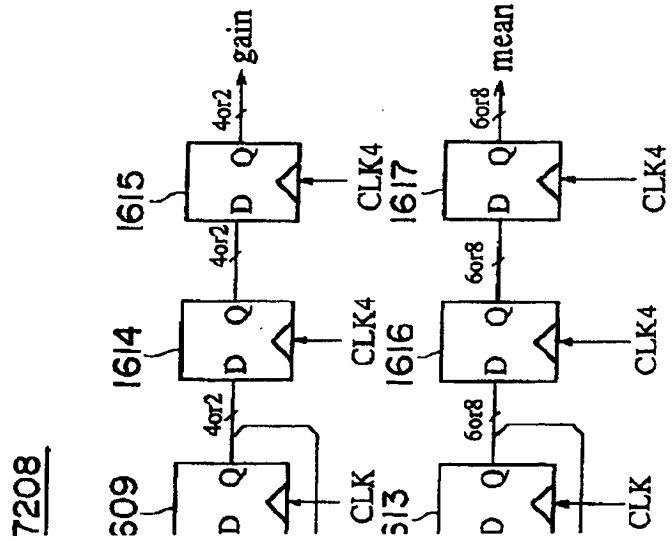

[Drawing 29]

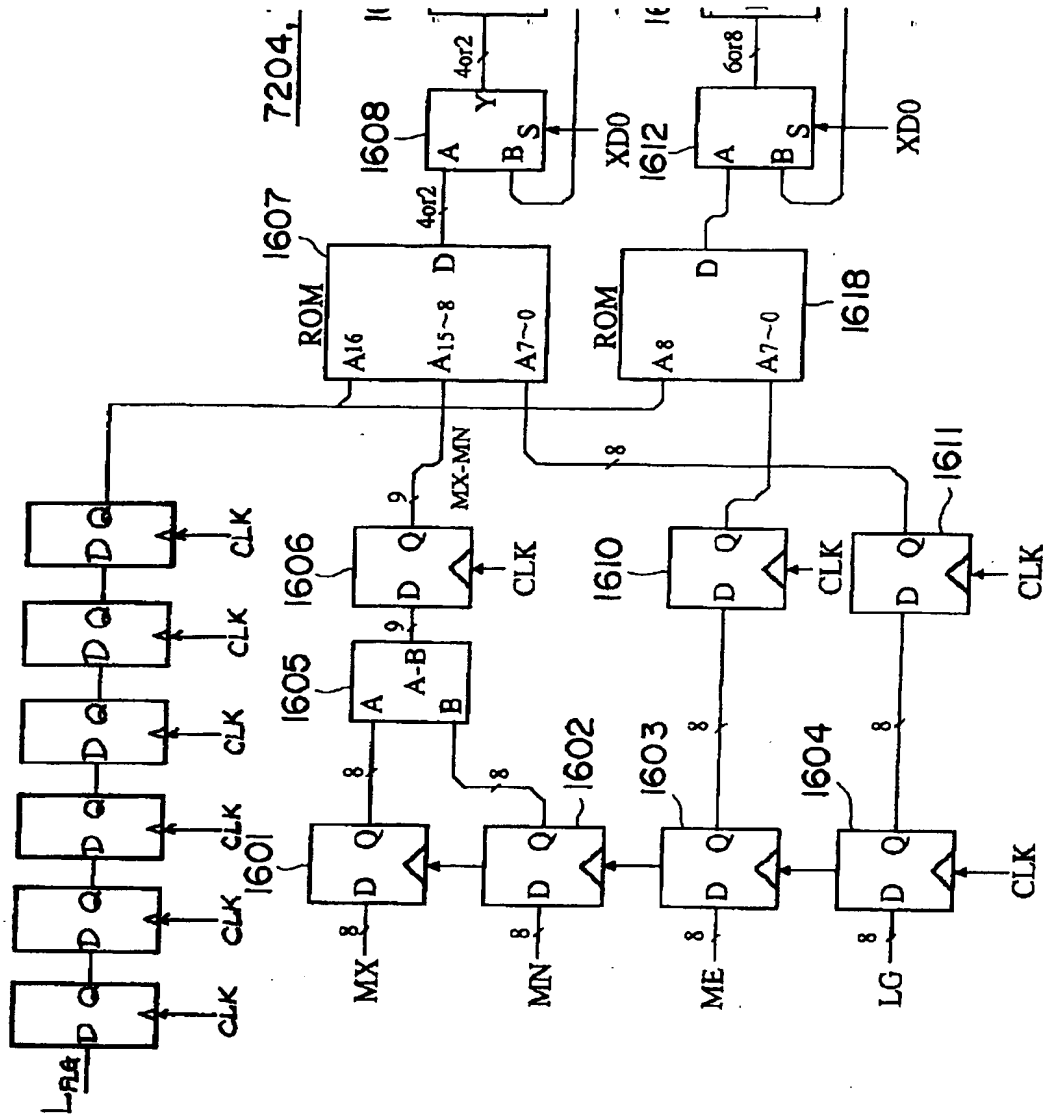



[Drawing 17]

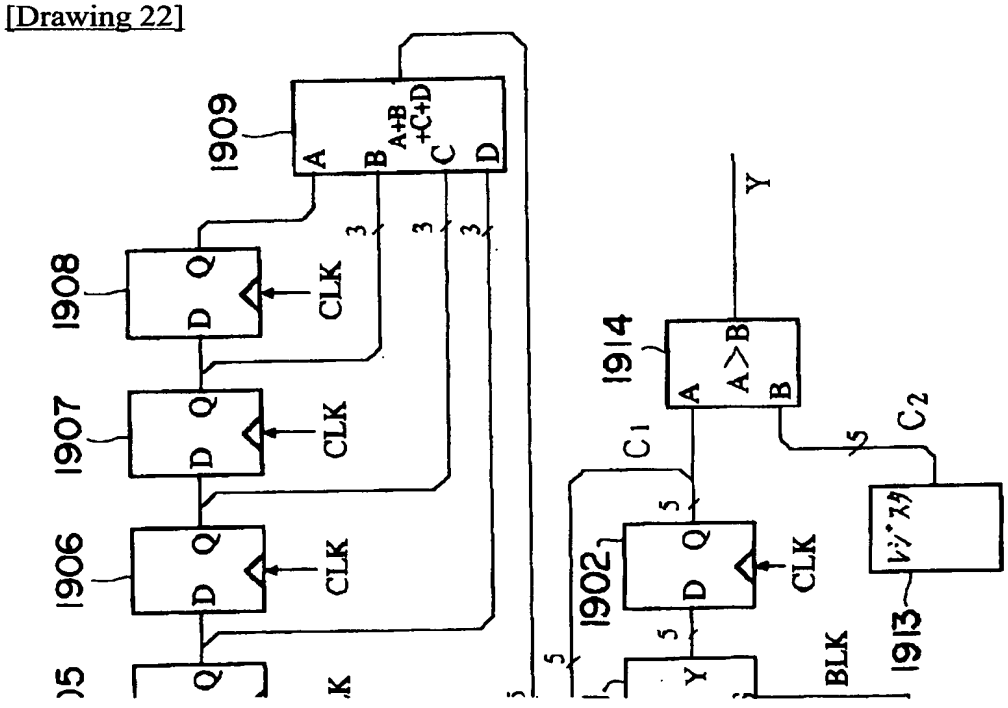

1501
1502
1503
1504
1505
1506
7204,7208
A
B
C
D
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
8
D
Q
A
B
C
D
S
Y
1525
9
LMX (3~2)
1526
10
LMN (3~2)
1551
A+B+C+D
4
11
2
全てのフリップ
フロップへ
CLK

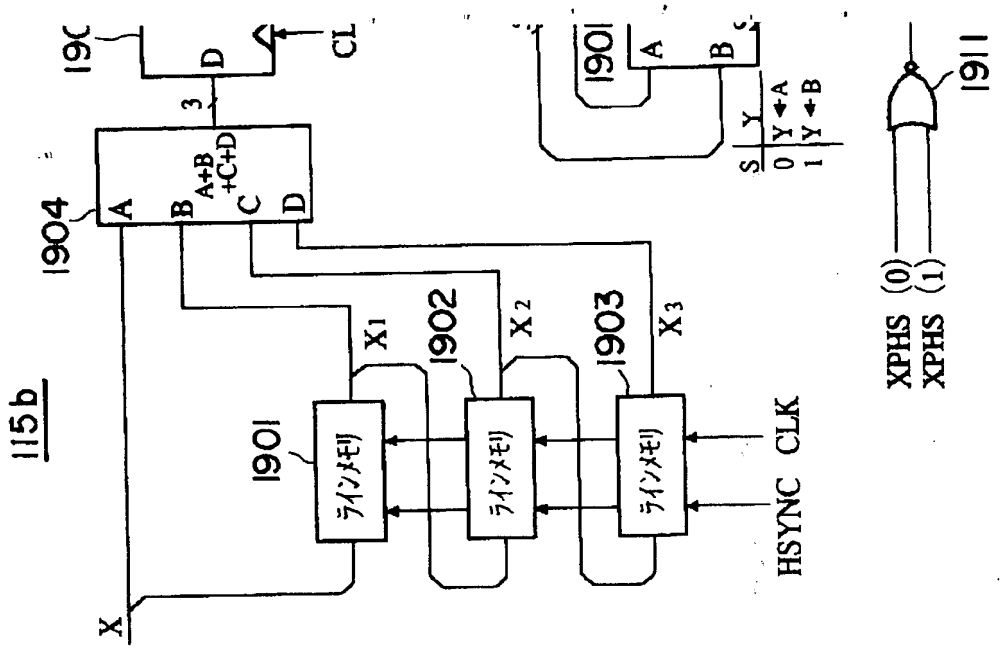
[Drawing 19]


gain
mean
4or2
6or8
1615
1617
1614
1616
609
613
7208
CLK4
CLK
D
Q

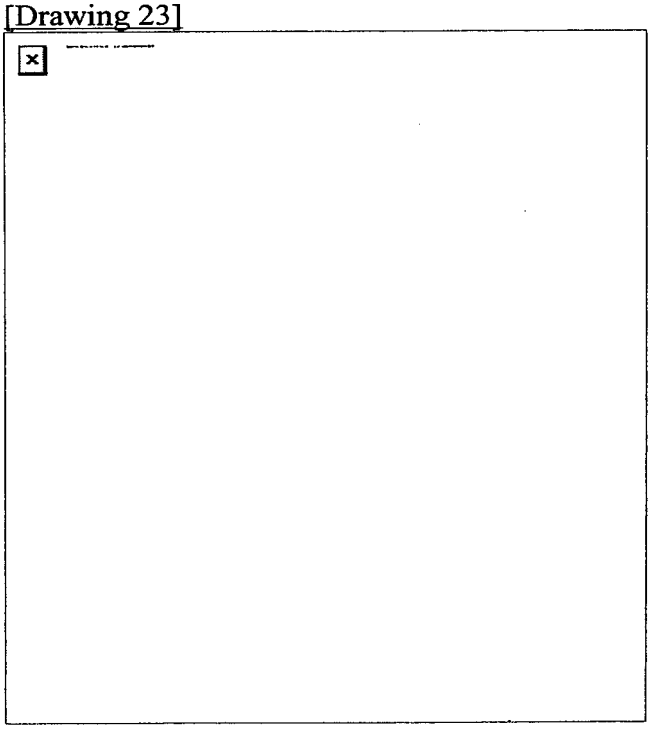

7204
1608
1612
1607
1618
1606
1610
1611
1605
1602
1603
1604
1601
ROM
A16
A15~8
A7~0
A8
A-B
MX-MN
CLK
XD0
4or2
6or8
MX
MN
ME
LG

[Drawing 22]

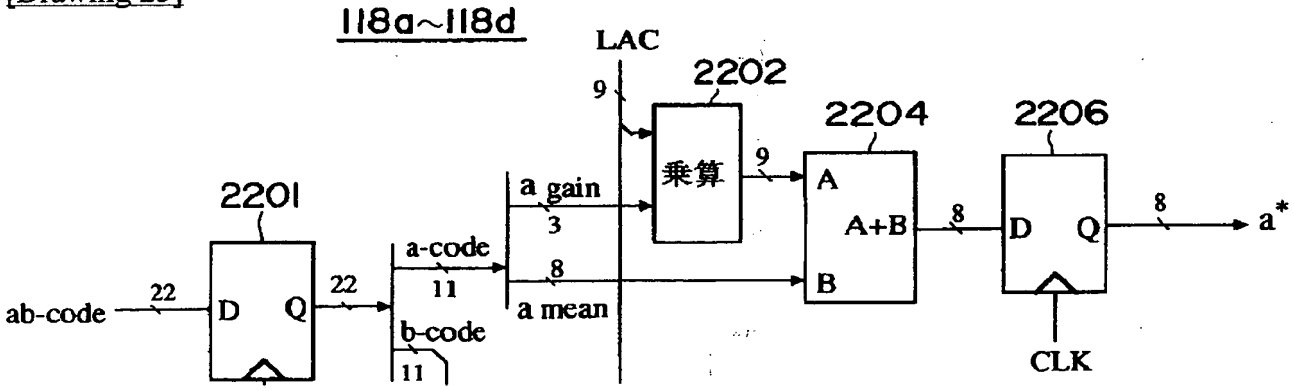

1909
A+B+C+D
1908
1907
1906
1914
A>B
1902
1913
CLK
C1
C2
BLK
Y

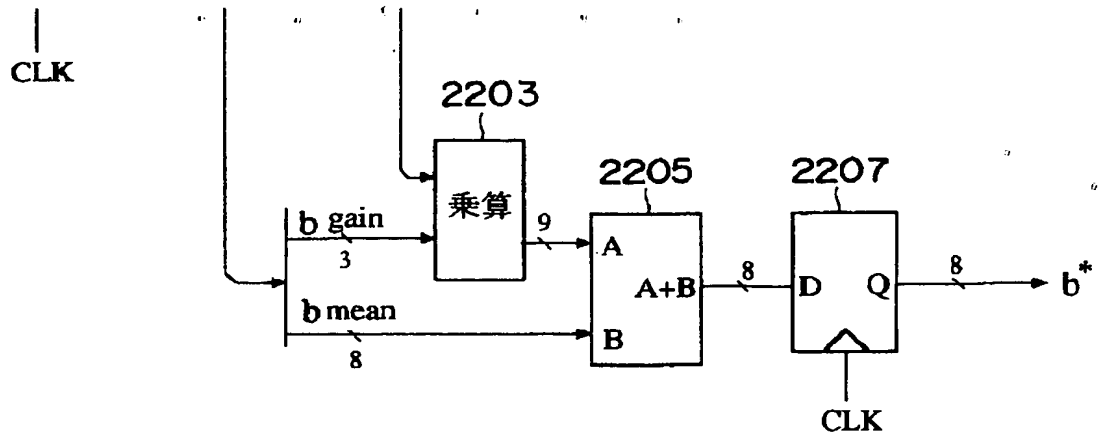



[Drawing 23]

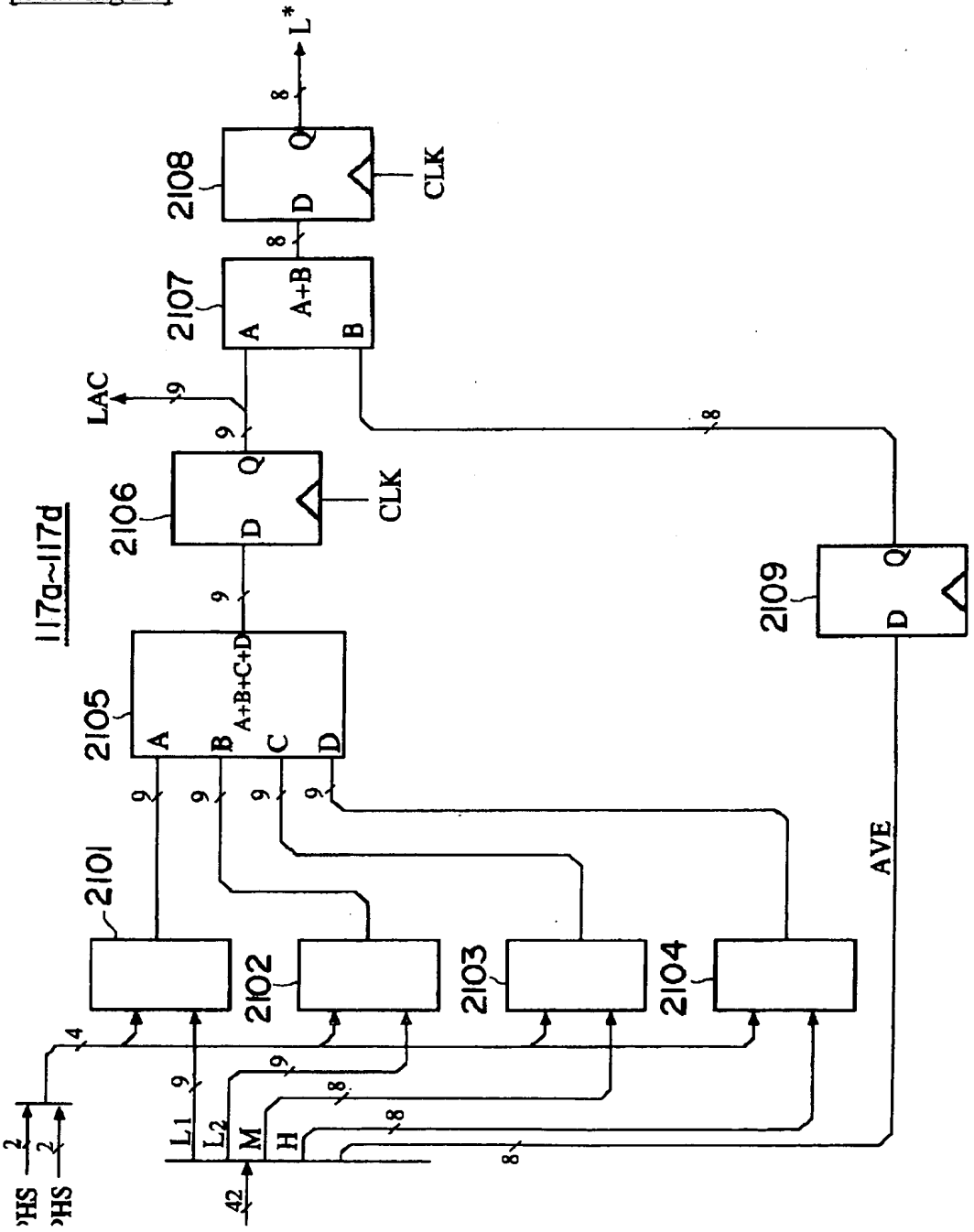


[Drawing 25]



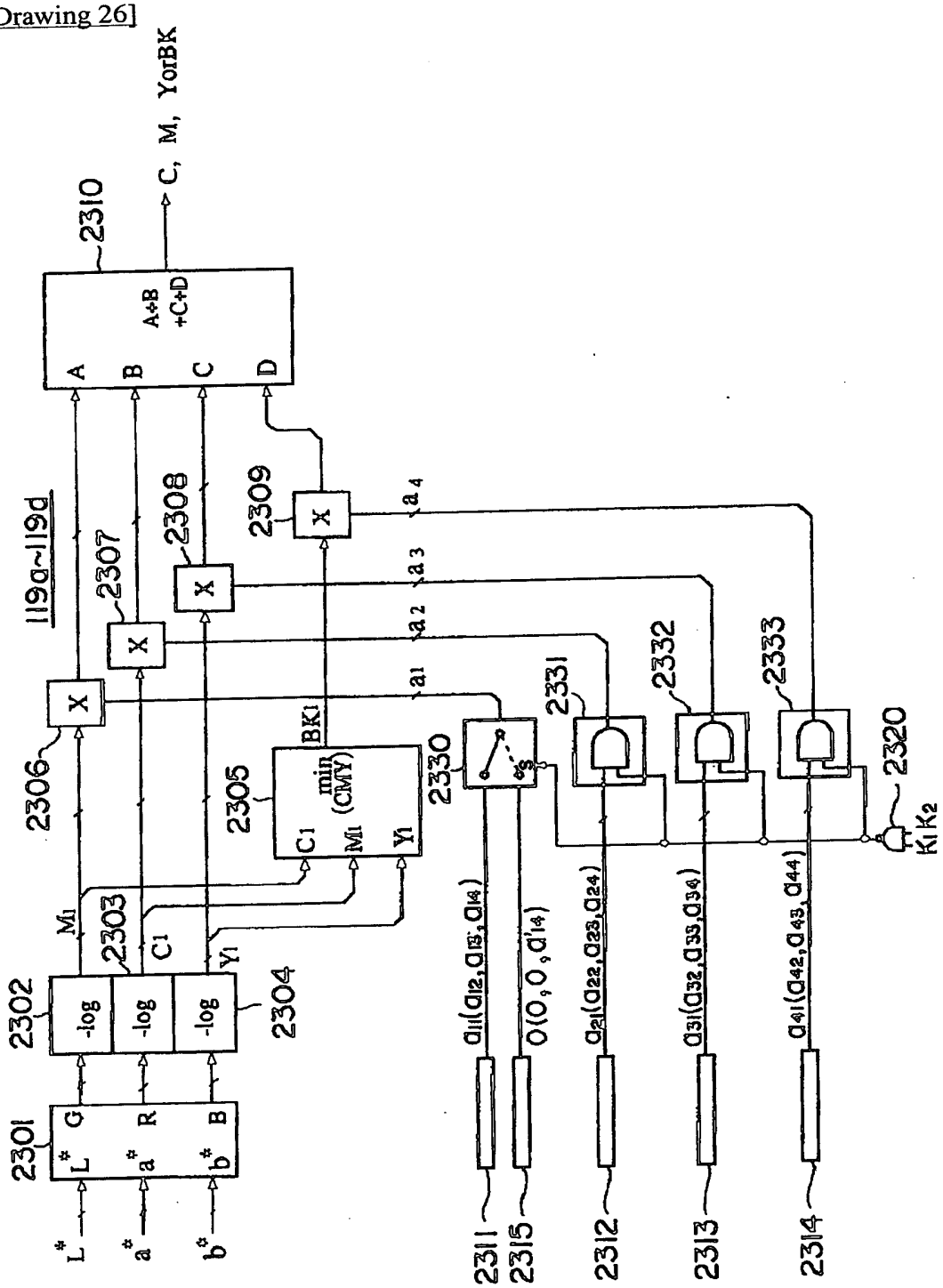

CLK
2203
乗算
b gain
3
9
2205
A
A+B
B
8
2207
D
Q
8
b*
b mean
8
CLK

[Drawing 24]


L*
8
2108
Q
D
CLK
8
2107
A
A+B
B
LAC
9
9
8
2106
Q
D
CLK
117a~117d
9
2109
Q
D
2105
A
B
A+B+C+D
C
D
9
9
9
9
2101
AVE
2102
2103
2104
4
9
9
8
8
8
2
2
L1
L2
M
H
42
HS
HS

YF XI code

[Drawing 26]

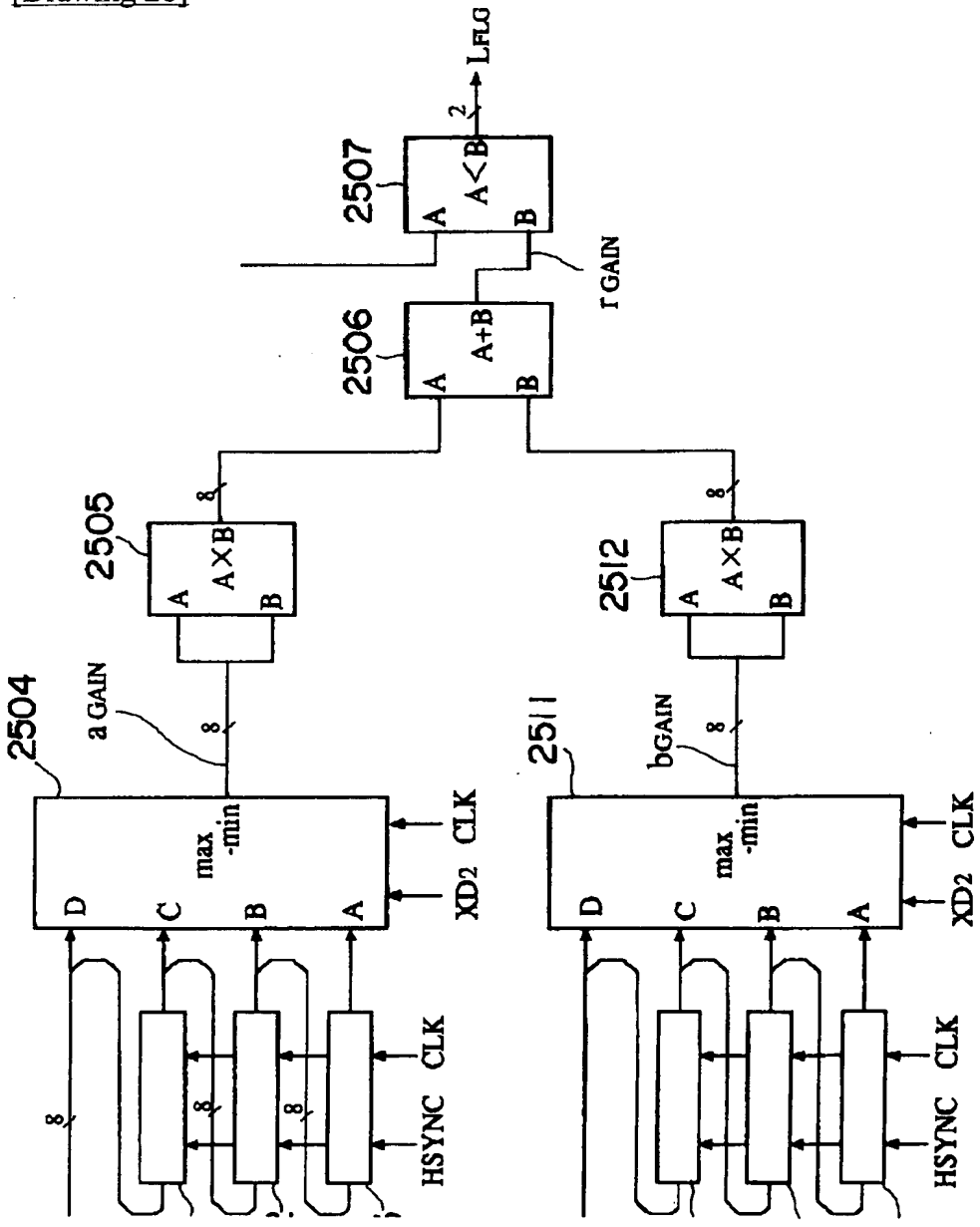


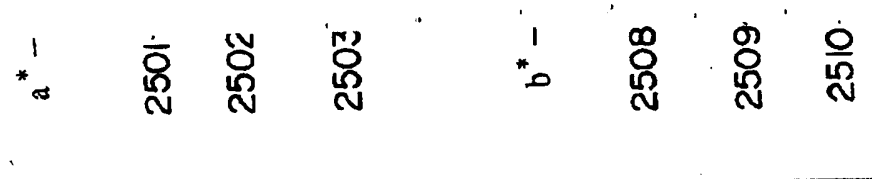

[Drawing 27]

| K1∩K2 | 現色 | a1 | a2 | a3 | a4 | 備考 |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | M | $a_{11}$ | $a_{21}$ | $a_{31}$ | $a_{41}$ | 非黒文字部ﾏｾﾞﾝﾀ現像 |
| | C | $a_{12}$ | $a_{22}$ | $a_{32}$ | $a_{42}$ | 非黒文字部ｼｱﾝ現像 |
| | Y | $a_{13}$ | $a_{23}$ | $a_{33}$ | $a_{43}$ | 非黒文字部ｲｴﾛｰ現像 |
| | Bk | $a_{14}$ | $a_{24}$ | $a_{34}$ | $a_{44}$ | 非黒文字部ﾌﾞﾗｯｸ現像 |
| 1 | M | 0 | 0 | 0 | 0 | 黒文字部ﾏｾﾞﾝﾀ現像 |
| | C | 0 | 0 | 0 | 0 | 黒文字部ｼｱﾝ現像 |
| | Y | 0 | 0 | 0 | 0 | 黒文字部ｲｴﾛｰ現像 |
| | Bk | $a'_{14}$ | 0 | 0 | 0 | 黒文字部ﾌﾞﾗｯｸ現像 |

[Drawing 28]






[Translation done.]